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ADVANCED SILICON TECHNOLOGY FOR MICROWAVE CIRCUITS

Final Contract Report

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Microelectronics

Naval Research Laboratory
Contract No. N00014-91-C-2313

March 8, 1994

Westinghouse STC
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ABSTRACT

MICROX is a silicon-on-insulator (SOI) technology using high resistivity (>3,000 ohm-cm) silicon substrates to integrate RF and digital circuits. Channel length (down to 1/4 μm) and gate arrangement influences on frequency, power, and noise performance of FETs were characterized. Processing steps for MICROX MMICs (Miniature Microwave Integrated Circuits) were identified and developed. The best MICROX power result was 250 mW per mm of gate periphery (8.45 dB of associated gain, 49% Power Added Efficiency [PAE]) at 2 GHz from a non-LDD device (gate length of 0.55 μm). At 10 GHz an LDD FET (gate length, 1/4 μm) delivered 60 mW/mm of power (PAE, 19%; gain, 4.6 dB). The best broad-band noise figure (non-LDD FET; gate length, 0.48 μm) was 0.8 dB with 17.7 dB of associated gain at 2 GHz. These results are superior to those reported for alternative types of high frequency silicon FETs. Demonstration circuits (several L/S band amplifiers, a multi-bit attenuator, and a FET mixer) were selected, designed, simulated, and implemented in MICROX. MICROX provides higher frequency capability than alternative silicon approaches by eliminating parasitic capacitances associated with low resistivity bulk silicon. With silicon IC fabrication methods, MICROX offers a reduced risk route to high volume, low cost manufacturing of RF and high speed digital ICs, compared to GaAs.

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ACKNOWLEDGMENTS

It is a pleasure to acknowledge contributors to the concepts, identification of special topics, and fabrication efforts which were applied on this program. H. C. Nathanson, Westinghouse STC, originated the MICROX concept which combines the features of a silicon-on-insulator structure with a microwave-enabling, high resistivity substrate. I. Lagnado, NOSC, helped to focus attention on the distinctions between power and digital processing geometries which affect thermal consideration in SOI devices. H. B. Dietrich, NRL, suggested making the technology capability comparisons covering GaAs FETs and HEMTs and Si FETs. R. R. Papania, was instrumental in the progress of this program by scheduling the time of his support team members (P. Kost, G. D. Griffith, J. T. McAdams, S. Maystrovich, R. P. Sadusky, J. L. Sotkowski, and H. J. Stoutmire) for the device and circuit fabrication effort. Especially appreciated were the extra efforts by R. J. Fiedor, J. C. Kotvas, R. A. Madia, J. R. Morris, D. W. Peters, M. J. Testa, W. J. Toth, and W. F. Valek in co-ordinating time-critical, multiple step processes for capacitor dielectrics, electron-beam and optical lithography, vias, and electroplating. A. J. Riding, Westinghouse Baltimore, arranged for thinning of wafers prior to via processing.

1. SUMMARY

MICROX is a silicon-on-insulator (SOI) technology which employs high resistivity (>3,000 ohm-cm) silicon substrates, for integrating RF and digital circuits. It offers higher frequency capability than conventional silicon technology which utilizes low resistivity (<10 ohm-cm) bulk silicon and junction isolation of devices. MICROX eliminates significant substrate parasitic capacitances, thus providing higher frequency capability for a given gate length and set of design rules, than bulk silicon. As a silicon technology, MICROX has the potential for implementing RF and high speed digital circuits at low cost.

On this program the approach was to adapt the design information base on GaAs linear FETs and RF circuits to MICROX use. Existing silicon and GaAs processes were modified and new procedures were developed to meet MICROX fabrication needs. The processing steps developed for MICROX MMICs included: planarization, salicidation, gate realignment and metal reinforcement, capacitor dielectric formation and rejection, airbridge fabrication, wafer thinning, and via preparation. This effort has shown the feasibility of fabricating MICROX MMICs (Miniature Microwave Integrated Circuits) using Si IC processing methods. Demonstration circuits, including several amplifiers, a multi-bit attenuator, and a FET mixer, were selected, designed, simulated, and implemented in MICROX.

The benefits and limits of short gate geometries (down to 1/4 μm) were explored as regards FET performance. Influences of channel geometry and gate arrangement on frequency, power, and noise performance of MICROX FETs were characterized. MICROX device results were compared to the latest available silicon and gallium arsenide ones as regards DC, RF and noise performance. The best MICROX power result was 250 mW per mm of gate periphery (8.45 dB of associated gain, 49% Power Added Efficiency [PAE]) at 2 GHz from a non-LDD device (gate length of 0.55 μm, 4 x 100-μm gate structure.) At 10 GHz a Low Doped Drain (LDD) FET with a gate length of 1/4 μm delivered 60 mW/mm of power and had PAE of 19% with an associated gain of 4.6 dB.

The best broad-band noise performance was for a non-LDD FET (gate length of 0.48 μm, 6 x 30-μm gate structure) which had a noise figure of 0.8 dB, with 17.7 dB of associated gain at 2 GHz. These noise results are better than those reported for other silicon devices of comparable frequency capability. BESOI (Bonded and etched Back Silicon on Insulator) FETs have been reported with minimum noise figures of 5.0 dB at 2 GHz (associated gain of 6.4 dB). Bulk NMOS devices on a 50 ohm-cm substrate have been reported with a minimum noise figure of 5.3 dB at 8 GHz (about 2.2 dB higher than for MICROX) and an associated gain of 4.6 dB (3.4 dB lower than for current MICROX).

GaAs devices are usually considered as the basis for implementing most MMICs due to their power capabilities and their low noise characteristics. For microwave power uses GaAs MESFETs hold a strong position. Recent advancements in HEMTs have raised their high frequency power capability above that of GaAs FETs. Issues of fabrication difficulty and performance variability remain to be addressed in connection with large-scale manufacturing efforts incorporating HEMTs. The results of this program show that silicon MICROX FETs, although limited to lower power and frequency capability than GaAs FETs or HEMTs, have power and noise performance which make them attractive for many cost-sensitive MMIC applications.

Si MOSFET circuit analogs to some GaAs MMICs are presently realizable, with the junction-isolated designs on which conventional digital MOS circuits are based. They are expected to displace silicon bipolar and GaAs MESFETs in transceiver-type applications, such as L- and S-band amplifiers and mixers, as scale-up manufacturing efforts are undertaken to affordably fulfill the performance needs of these applications. The junction-isolated approach will exploit silicon capabilities for high voltage long drain FETs, low substrate thermal resistance, and 200 C junction operating temperatures. MICROX can provide the same features, while offering higher frequency capability for a given gate geometry, due to the elimination of key parasitic capacitances associated with low resistivity bulk silicon. For the high frequency applications to which it is suited, MICROX can draw directly on silicon IC fabrication capability, offering an advantage over GaAs in a reduced risk route to high volume, low cost manufacturing of RF and high speed digital ICs.

2. INTRODUCTION

As this program began, there was a concurrent industry interest in exploring various types of silicon MOS field effect transistors for microwave uses. Successful microwave application of semiconductor devices faces the challenge of reducing parasitic effects to avoid overwhelming the active device behavior. For this program the Westinghouse approach has been to use MICROX, based on a high resistivity silicon substrate having a Silicon-on-Insulator structure, for FETs with aggressive microwave geometries. These MICROX FETs benefit from reduced substrate capacitance and are silicon analogs to GaAs FETs used in MMIC (Miniature Microwave Integrated Circuit) applications. Substantial program effort has been applied to understand device structure and fabrication influences on microwave performance and to utilize that knowledge in designing MMICs which demonstrate the usefulness of MICROX.

2.1 Program Objective and Tasks

The objective of this program is to use MICROX, a silicon-on-insulator (SOI) technology with high resistivity (>3,000 ohm-cm) silicon substrates, for integrating RF and digital circuits. For this program, the goal is to have MICROX provide affordable functions for future radar systems, particularly in phased array transmit/receive modules. There are three tasks on this program:

Task 1 - Increase the frequency limits of MICROX microwave FET performance as gate lengths are reduced to 0.25 micron, and explore means for increasing the power of such FETs.

Task 2 - Demonstrate a distributed amplifier for 1 to 10 GHz applications using MICROX FETs.

Task 3 - Demonstrate key L-band radar receiver circuits in silicon

Subtask details and the program schedule are shown in Figure 1. A list of program milestones (identified by number for the program subtasks in Figure 1) is given in Table 1.

2.2 Comparison of Major Semiconductor Capabilities

As stated in Section 2.1, the aim of this program is to consider the prospects of using silicon for advanced microwave circuits, particularly by taking advantage of recent developments in MICROX, a

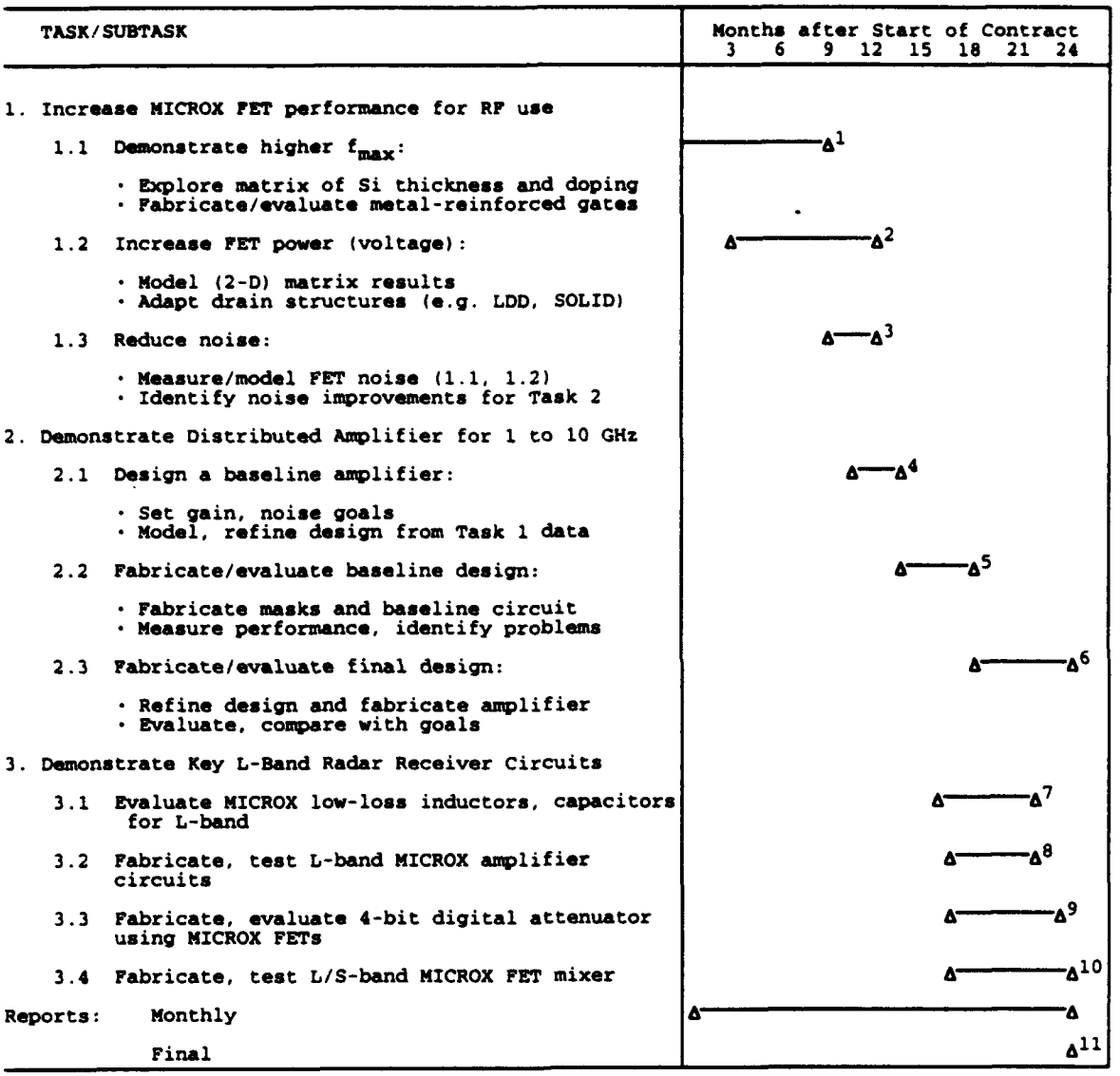

Figure 1. Program schedule with sub-task details. Numbered milestones are listed in Table 1.

Table 1. LIST OF PROGRAM MILESTONES

Number	Description	Expected Completion
1.	F_{max} of 20 GHz demonstrated.	(6/31/92)
2.	Drain-to-source voltage of 10 V achieved.	(9/31/92)
3.	Sources of noise identified, ranked.	(9/31/92)
4.	Baseline distributed amplifier design complete.	(10/31/92)
5.	Baseline distributed amplifier evaluated.	(12/31/92)
6.	Distributed amplifier characterized.	(9/30/93)
7.	L/S-Band MICROX passive components evaluated	(7/31/93)
8.	2-, 3-stage amplifiers compared through 3 GHz	(7/31/93)
9.	L-Band digital attenuator characterized	(8/31/93)
10.	L/S-Band MICROX FET mixer evaluated	(9/30/93)
11.	Draft of final report delivered.	(9/30/93)

silicon-on-insulator (SOI) approach using a very high resistivity substrate. To put the results of this program in perspective, this section gives an overview of Si, GaAs, and advanced semiconductor device performance capabilities and application opportunities. Another important issue, assessment of the factors which affect the commercial viability of both MICROX and GaAs technologies, is treated in Section 2.3.

Recently, interest has developed in silicon MOS field effect transistors for microwave applications. The possible use of silicon devices for microwave integrated circuits is not new. Pucell[1] recounts that the first U. S. government program to use semiconductors in radar transmit/receive modules began in 1964, exploring silicon microwave integrated circuits fabricated in high resistivity substrates. Although the initial substrate characteristics were adequate to support microstrip transmission lines, the program was unsuccessful because the high substrate resistivity could not be maintained throughout the high temperature cycles required for device and circuit fabrication.

Extensive efforts to resolve the silicon substrate problems were not undertaken, probably because of the successful application of GaAs devices in microwave circuits. Mehal and Wacker[2] employed semi-insulating GaAs as a substrate for Schottky barrier and Gunn diodes to implement a 94 GHz front end. Pucell cites the demonstration by Pengelley and Turner[3] of an X-band amplifier using GaAs FETs in 1976 as the beginning of work on GaAs MMICs (miniature microwave integrated circuits). Since then, designers and developers have exploited gallium

arsenide for the low microwave loss of its semi-insulating form, for the ability of its Schottky barrier gate FETs to implement both high efficiency and low noise amplifiers (as well as mixer circuits with gain), and for unique devices such as variable gain, dual gate FETs which are amenable to either analog or digital control.

As both silicon and gallium arsenide device and circuit technologies matured, they satisfied distinct needs. Silicon generally was used in such digital applications as large scale and personal computers and in linear RF circuits for communications and entertainment equipment well below 100 MHz. Gallium arsenide served microwave needs, particularly military ones, above 1 GHz. Silicon bipolar transistors filled RF application niches below 1 GHz.

Recent performance advances in both silicon and gallium arsenide technologies have caused their capabilities to overlap as regards microwave and digital applications. The aim of this program is to assess the microwave capabilities of silicon, by exploiting its MICROX form for a variety of SOI-related high frequency benefits. A survey of the current status of FET technologies as regards microwave power and noise is summarized in Tables 2 and 3, including key results from the current program. To focus on useful microwave power, the second column of Table 2 gives the maximum power at the 1 dB compression point, corresponding to the onset of output power saturation. Relevant details of the conditions for each maximum power example are given in the next three columns. The next column indicates the short-circuit current gain cut-off frequency (theoretically proportional to transconductance ÷ gate-to-source capacitance or to saturated carrier velocity ÷ gate length). Gate length and width are indicated in the seventh column.

For microwave power applications GaAs MESFETs hold an undeniable position in terms of demonstrated performance and breadth of application, particularly in MMICs. Until recently HEMTs have been limited to unit power levels similar to GaAs FETs, and have been less attractive for most applications due to their fabrication difficulty and performance variability. Processing improvements have changed this outlook somewhat, as shown in Table 2, with the increased HEMT power deriving from higher current capability, rather than increased voltage. Ultimately the greater fabrication complexity of HEMTs must be amenable to cost-effective, large-scale manufacturing if they are to replace GaAs FETs for power. Silicon FETs of the MICROX type, the last entries in Table 2, have lower power and frequency capability than GaAs FETs or HEMTs, reflecting the lower values of carrier saturation velocity (by a factor of at least 2) and breakdown field in silicon compared to GaAs. Nevertheless, silicon devices will benefit due to design improvements from the GaAs FET area and from direct application of low-cost, high volume silicon IC fabrication methods.

Table 2. SUMMARY OF RF POWER EXAMPLES FOR GaAs- AND Si-BASED FET TECHNOLOGIES

Device Technology	Max. Power @1 dB comp. (mW/mm)	Meas. Freq.	Assoc. Gain (dB)	Power Added Efficiency	f_t	Gate Geometry	Comments
GaAs FET	400	18 GHz	9 dB	35%	Not given	0.3 μm x 0.6 mm	Ref. 4.
	355	18 GHz	8.5 dB	35%	Not given	0.3 μm x 1.2 mm	
HEMT	467	30 GHz	2.7 dB	20%	20 GHz	0.8 μm x 1.2 mm	Ref. 5.
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	808	10 GHz	10 dB	70%	33-42 GHz	0.25 μm x 1.2 mm	Ref. 6.
	808	18 GHz	6.8 dB	48%	33-42 GHz	0.25 μm x 1.2 mm	
- - - - - -	- - -	- - - -	- - - - -	- - -	- - -	- - - - - - -	- - - - - - - - -
	503	10 GHz	8.8 dB	76%	18 GHz	0.25 μm x 1.2 mm	Ref. 7.
Si MOSFET MICROX	250	2 GHz	8.5 dB	49%	24 GHz	0.55 μm x 0.4 mm	This work
	50	10 GHz	4.6 dB	19%		0.25 μm x 0.4 mm	This work

Table 3. SUMMARY OF NOISE RESULT EXAMPLES FOR GaAs- AND Si-BASED FET TECHNOLOGIES

Device Technology	Minimum NF (dB)	Measurement Frequency	Associated Gain (dB)	Gate Geometry	Comments
GaAs FET	0.8 dB	8 GHz	Not given	0.25 μm T-gate 300 μm width	Ref. 8.
HEMT	0.4 dB	8 GHz	15.2 dB	0.25 μm 300 μm width	Ref. 9.
Si MOSFET MICROX	0.8 dB	2 GHz	17.7 dB	0.48 μm 6 x 30 μm width	This work
	1.5 dB	8 GHz	10.0 dB	0.48 μm 6 x 30 μm width	This work
Si MOSFET BESOI 50 Ω-cm substrate	5.0 dB	2 GHz	6.4 dB	1.0 μm 2 x 60 μm (Center-fed)	Ref. 10.
Si MOSFET Bulk 50 Ω-cm Si substrate	5.3 dB	8 GHz	4.6 dB	0.5 μm 2 x 25 μm	Ref. 11.

Table 3 gives an comparison overview of broadband noise capabilities of GaAs FETs, HEMTs, and Si MOSFETs. The latter category includes results from the current work as well as published information on FETs made both with Bonded and Etched Back SOI (BESOI) and with moderate resistivity bulk substrates. According to Zimmermann and Salmer[12], the noise performance of HEMTs benefits significantly from their higher value of carrier drift velocity (up to twice that for GaAs FETs). Among the silicon MOSFETs in Table 3, the MICROX devices have advantages of short gate length and high gain. As with power considerations, improved MICROX FET noise performance is expected from design and process refinements.

The power and noise prospects of silicon MOSFETs are acceptable for many MMIC applications requiring low-cost manufacturing. Silicon bipolar technology has already established a beachhead for such applications. Snapp[13] provides a supplier's view of silicon MMICs and gigabit/sec digital ICs incorporating silicon bipolar transistors. He contends that they "have become established as the most cost-effective microwave semiconductor components for many high-volume and high-performance applications even at frequencies above 4 GHz." Snapp cites potential uses of Si MMICs in digital radio (LO/IF), direct broadcast satellite (LO/IF), navigation satellites, S-band radar, cellular radio, TV tuners and cable TV equipment, and IF stages in millimeter wave guidance systems for missiles.

In some applications where low-to-medium power capability is adequate, circuit analogs to GaAs FET MMICs using Si MOSFETs are acceptable, even in the junction-isolated form on which conventional digital MOS circuits are based. Camilleri et al.[14] expect junction-isolated, bulk silicon MOSFETs to displace silicon bipolar and GaAs MESFETs in transceiver-type applications, such as L- and S-band amplifiers and mixers. Their approach exploits key silicon capabilities for high voltage (28 V) long drain FETs, low substrate thermal resistance, and 200 C junction operating temperatures to implement MOSFET power and low noise amplifiers, mixers, and oscillators needed for affordable, low-power transceivers.

MICROX can provide the features of RF Si MOSFETs cited by Camilleri et al., offering higher frequency capability for a given gate geometry, due to the elimination of the junction/substrate and interconnect/substrate capacitances associated with low resistivity bulk silicon. MICROX devices will also provide performance improvements over bulk silicon MOS circuits in RF uses by eliminating leakage current from bulk junction isolation tubs. Recently digital signal processing methods have been applied to high frequency communications. Here MICROX offers a compound advantage of lower cost, by integrating both RF and digital portions of the circuitry in silicon, and of higher speed

digital circuits than can be obtained in bulk, junction-isolated silicon.

High speed digital circuits in gallium arsenide have been used for supercomputers, benefitting from the higher electron drift velocity and lower substrate parasitics compared to conventional silicon circuits. Greiling[15] compared speed and power capabilities of silicon bipolar, Si MOS, and various GaAs FET approaches for implementing high speed multipliers, gate arrays, and memories. In the first two applications, GaAs provided about a factor of 3 speed advantage compared to silicon; but (at the level of 1985 technology which was being evaluated) the GaAs parts were only about 1/4 as complex as the Si ones. In high speed memories, the factor of 3 in speed improvement for GaAs over Si emitter-coupled logic (ECL) was maintained, but Si NMOS and CMOS memories were only slightly slower than GaAs for the same dynamic power per gate.

Gourier[16] lists several important drawbacks to GaAs for digital applications. Sidegating problems associated with traps and poorly passivated surfaces in GaAs require that individual devices be less densely packed than in silicon. Device uniformity and power dissipation considerations at the chip level limit the integration density or complexity of digital GaAs to between 1/100 and 1/1000 of that for Si. In realizing hardware, architectural means can be used to accommodate this integration restraint and exploit GaAs speed benefits, but as relatively small GaAs chips proliferate, assembly and packaging costs rise. For the near future, large volume supercomputer-type high speed uses are not likely to fuel a sufficient demand for gallium arsenide digital parts to support the needed development of a low cost digital chips manufacturing capability, of the kind already in place for silicon ICs.

In addition to the strong competition between GaAs and Si to meet RF and microwave needs in circuits and subsystems, particularly through L- and S-band, there are related advanced material/device possibilities, including Si/Ge heterojunction base transistors and AlGaAs-based HEMTs approaches, for supplying important enhanced capabilities in these applications. For the most part, contributions to the technical literature in these material and device areas focus on the detailed performance attributes of each approach. Usually the linking of performance and cost, which determines the economic prospects of a particular technology, is not considered.

2.3 Perspective: Performance and Cost Issues

Each of the semiconductor approaches considered in the preceding section has some some key performance strengths for high frequency or high speed applications. In the past, extensions of either Si or GaAs

technology to new applications were justified on technical capabilities alone. Such justifications may be appropriate for limited niche applications. For wide utilization of integrated circuits in both military and commercial areas, current criteria focus on providing acceptable performance at an affordable cost. Cost issues, as much as speed capability, play a key role in determining the growth potential and ultimate pervasiveness of a commercially-viable semiconductor technology. Cost considerations, favorably impacted by high volumes and batch handling capability, have made silicon dominant in most digital and audio-to-low-RF analog applications.

The issue of affordability is the focus of Skinner's recent assessments of GaAs for RF and high speed digital uses.[17,18] Using costing methods originally applied to silicon products, he identifies conditions which GaAs must meet for commercial succcess. Skinner comprehensively reviews selected silicon examples, producing a cost-yield model and exploring successful manufacturing and application examples. He considers several GaAs devices and circuits, both RF and digital, and models the impact of throughput, yield, testing, and packaging on the final product cost. Finally, he suggests scenarios for the entry of GaAs into appropriate high volume applications.

Skinner gives projected best-case costs for GaAs and Si BiCMOS digital ASIC examples of $48 and $42, respectively. (The case of a smaller GaAs communications chip provides a perspective on MMICs as well.) For GaAs this optimistic target cost has two major requirements. Die sort yield must reach 60%, which is achievable if the defect density can be reduced from the current typical value of $5/cm^2$ to $1.5/cm^2$, the level for silicon. Additionally, processed wafers (100 mm diameter) must cost $510 or less. These targets will require lower starting substrate costs, reduced defect counts, and much higher process yields. Skinner assumes that facility utilization is 100% for these examples. GaAs, as well as many Si, ASIC operations commonly have low utilization levels, which ultimately increase the yielded wafer costs.

Since junction-isolated silicon technology was the benchmark for Skinner's comparison, the Si (and MICROX) costs should be currently realizable, with some qualification. The preparation of airbridges, not a mainstream process in high volume IC manufacturing, is similar to that for commonly used multilevel interconnections. Additionaly, formation of 1/4-μm gates for MICROX MMICs, whether by electron beam or optical methods, will require manufacturing technology advancements. The availability and cost of large diameter SOI wafers and the reduction of function-killing defects associated with the oxygen implantation process are issues which material suppliers should resolve favorably to meet the market opportunities afforded by production volumes.

3. PROGRAM PLAN

The approach for this program was to understand and adapt the design information base for GaAs RF FETs and circuits to silicon MICROX. A major part of the effort was to demonstrate the suitability of existing or suitably modified silicon processes for device and circuit fabrication. It was recognized that key silicon and GaAs processes would require adaptation and modification to meet the fabrication needs of silicon RF circuits and of silicon-on-insulator (SOI) structures. Since achieving good microwave performance in MICROX was critical, exploring the benefits and limits of short gate geometries on FET performance was important in the first part of the program. In order to provide a convincing demonstration of MICROX utility, relevant demonstration circuits were to be identified and implemented in MICROX.

3.1 FET Designs

The background for this program combined the areas of GaAs FET designs and processing with silicon MOSFET technology. As a result of that background, emphasis was originally placed on five design issues:

(1) use of thin (about 10 nm) gate oxides,

(2) definition of short (0.25 micron) polysilicon gates,

(3) producing gates with low resistance (through the gate) by doping the poly-Si and forming titanium silicide contacts to it,

(4) lowering the resistance along gate fingers by using metal reinforcement of the gate, and

(5) reducing the resistances between the active channel and the source and drain contact regions.

Details of the device geometry exert a strong influence on frequency, noise, and voltage performance. For this program our approach was to use multi-fingered structures and a matrix to provide ranges of gate lengths, gate finger widths, and numbers of gate fingers. Devices with these variations were evaluated. The measurement results were fitted to equivalent circuits for devices. Geometric influences were characterized and used to create a scaling model on which designs of specific devices for circuit applications could be based.

3.1.1 Grounded Source FETs

Grounded source FETs were emphasized on the program. This configuration is commonly used for device development and modelling purposes. Figure 2 shows a schematic, plan view of a multiple gate, grounded source MICROX FET, provided with contact pads to facilitate RF evaluation using microwave probing methods. The airbridges for the source contact islands are not shown. Details of a single element of the device structure, with one gate finger between the airbridged source region (left) and one finger of the grain (right), are indicated in Figure 3.

There are several trade-offs between the silicon RF MOSFET structure and the RF GaAs FET structure. The silicon FET uses an oxide-insulated gate structure, rather than a Schottky barrier (SB). The primary advantages of such a structure over the SB are lower dc dissipation and the ability to modulate the maximum FET transconductance with positive gate voltage in the case of n-channel FETs. For SB gate GaAs FETs, the maximum transconductance is limited by the active layer thickness and doping, which are set early in the fabrication process.

The gate structure advantages in the silicon MOSFET require a more complex fabrication procedure. A thin gate oxide (about 10 nm thick) must be grown, then polycrystalline silicon must be deposited, appropriately doped, and defined lithographically. An intervening arsenic implantation may be done to form the lightly doped drain, shown in Figure 3, for higher voltage capability. Silicon nitride sidewalls must be formed to separate the source/drain and gate silicide regions. Finally, reinforcing metal must be defined along the width of the gate fingers to provide low RF resistance. This last metallization step is approximately equivalent to formation of the SB gate in a GaAs FET.

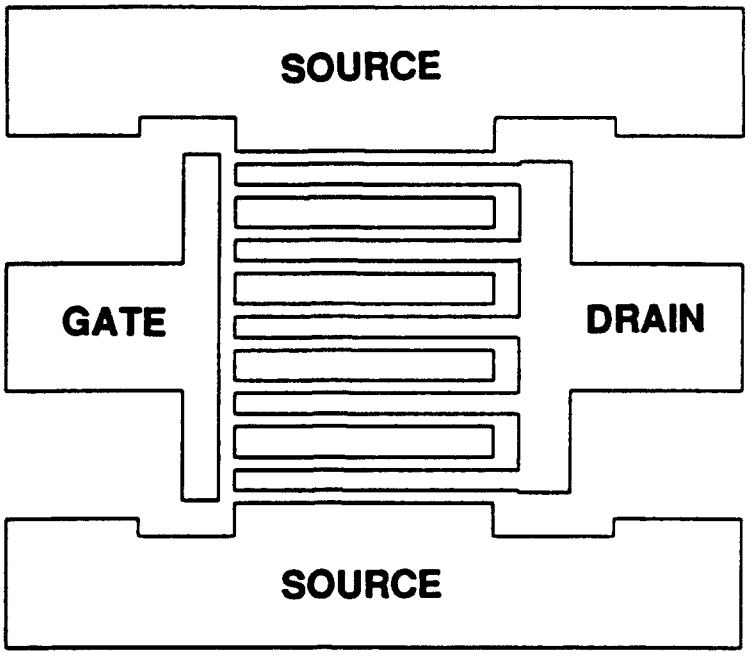


Figure 2. Plan view of a typical grounded source structure used for evaluating RF performance of MICROX FETs.

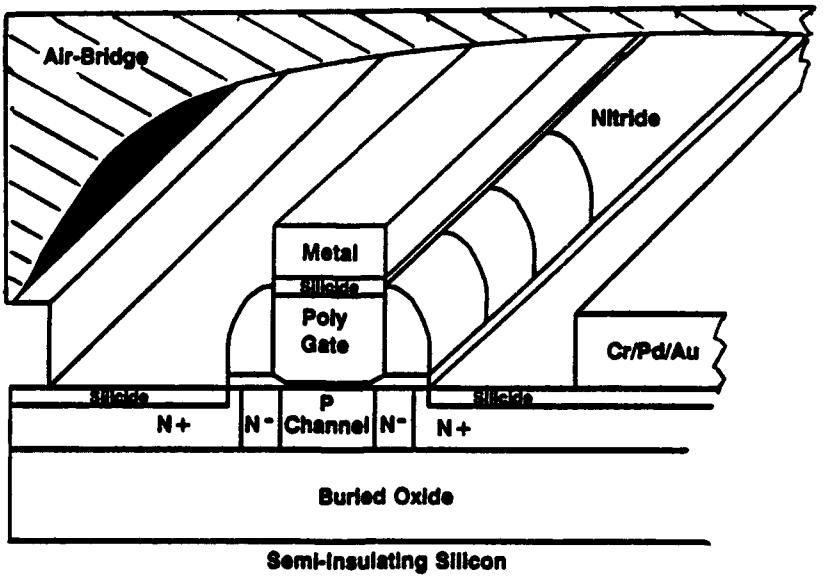


Figure 3. Schematic view of one segment of a MICROX FET, with the airbridged source at the left. Nitride sidewalls on the gate allow simultaneous silicide processing for the short 8gate and the source/drain regions.

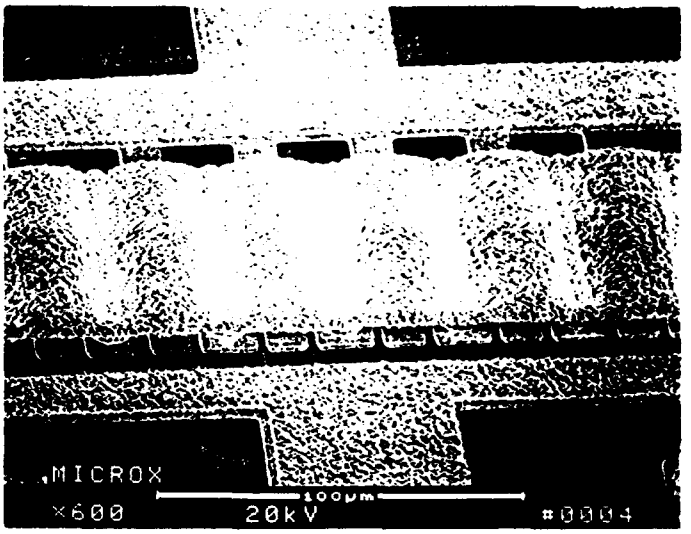


Figure 4. SEM view of a MICROX RF FET, with the airbridged sources in the center, and the drain and gate busses at the top and bottom, respectively.

The scanning electron microscope (SEM) view of a completed, common source MICROX FET in Figure 4 shows the multi-fingered gate structure (with the main gate buss at the bottom) and the airbridged contact to the individual source metallization regions.

Experience gained in developing microwave FETs in GaAs, at Westinghouse and within the industry, has underscored the importance of device design in minimizing parasitic resistance and capacitance effects. A controlling factor is the geometry with which the basic FET element is replicated to realize the current capability and impedance of the device. In order to provide an empirical data base for evaluating these effects, we have used a geometry variation approach as shown in Figure 5. The basic device array shown in this figure covers a two order of magnitude range in gate perimeter types (40 μm to 4000 μm). At each of 12 locations on the process development wafers, the array of gate types for n-channel accumulation-mode FETs was used at six sites. (Figure 6 shows 25 sites at one location. Two sites contain circuit and process test structures. The remaining sites are for experimental devices such as grounded gate FETs and p-channel FETs.) For each site, electron beam exposure of the gate was done to produce a desired, fixed gate length. From site to site, the exposure was varied to produce a different, fixed gate length, which ranged from 279 nm to 480 nm. This geometrical variation produced nearly two hundred FETs of each gate length for evaluation on each wafer. In this way, it was possible to characterize the device processing details (which varied from wafer to wafer) for influences on performance, particularly RF behavior, of a wide variety of device structures.

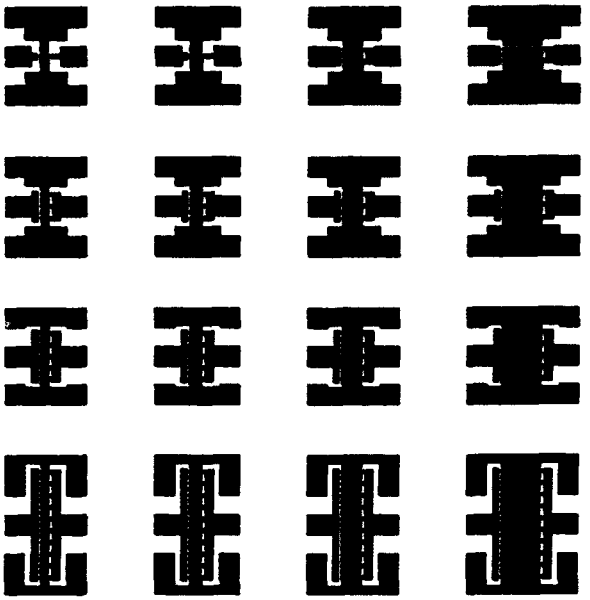


Figure 5. Detail of the FET contact metal mask design, showing 16 different gate types (each with a different number and width of gate fingers) for which a specific gate length was produced by electron beam exposure.

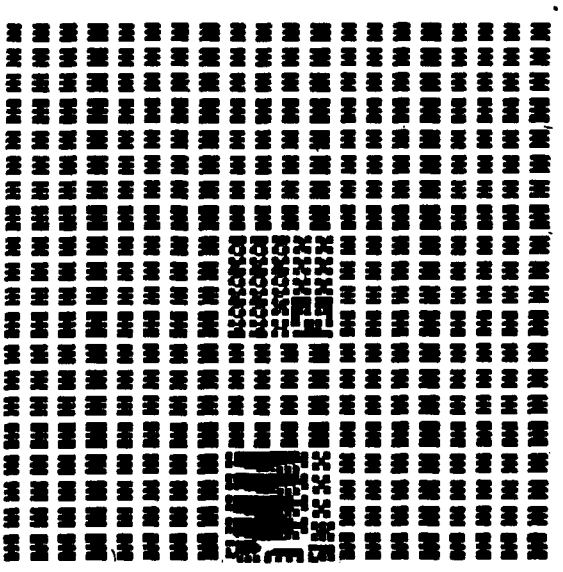


Figure 6. A view of the FET contact metal mask pattern applied at 12 locations over the wafer. At each location six different gate lengths (280 to 480 nm long) were produced, using E-beam exposure. Two of the sites contain test patterns instead of FETs.

On the basis of measurements and modelling related to the initial investigation of grounded source FETs, the MICROX demonstration circuits, described in Section 3.3, were designed. As a part of the approach to monitor processing effects, as well as to provide an expanded design data base, similar provisions were taken to vary device geometry of common source FETs in those wafer lots as well.

There were two major differences in the geometry variations which were used in the wafers with demonstration circuits. First, at each location on the wafer only 16 common source FETs were fabricated with the same basic width and gate finger arrangements as are shown in Figure 5. Second, the variation in gate length for the demonstration circuit wafers was made only as a function of the row position on the wafer, rather than being provided at each module site on the wafer, as was done in the initial case.

Other test structures were provided in the mask designs represented in Figure 6. In particular, provisions for common source p-channel MOSFET geometries were identical to those for the n-channel enhancement mode devices. These designs provided the first opportunity to critically evaluate the RF performance of silicon p-channel FETs. Forty-eight percent of the test FET array area was dedicated to these structures for the purpose of extracting scaled geometry information on MICROX FETs. The remainder of the area was used for other device structures, such as common gate designs, n-channel depletion mode devices (generally analogous to SB gate GaAs MESFETs), and process monitoring structures.

3.2 Processing Development

This program has addressed the identification and demonstration of key processes needed to fabricate Si RF MOSFETs and related components which are required in MMICs. Seven important areas of processing are considered:

- transferring silicon implantation and junction formation processes from digital to RF analog circuit applications,
- improving methods, especially in the case of SOI, for silicon surface planarization to accommodate the multiple, wide gate structures of RF FETs,
- adapting and incorporating GaAs-compatible passive component processing (especially for large area, Metal-Insulator-Metal capacitors and for plated inductors) to silicon,

- translating airbridge processing from GaAs to silicon practice,
- developing wafer thinning methods for stripline circuit applications of MICROX silicon,
- producing through-the-wafer vias to accommodate a back groundplane, and
- assessing the impact of material and processing non-uniformity issues on MICROX device and circuit producibility.

Adding to the challenge of addressing these major issues was the need to explore MICROX FET performance in the range of very short gate lengths, down to 1/4 micron, in order to guarantee performance for microwave applications. Many of the recent advances in the high frequency performance of silicon FETs have been a result of exploiting short gate geometries. That is part of the reason for making electron beam definition of short gates a key part of the present program. Additionally, the flexibility of an electron beam for direct writing of the gate pattern allows reliable achievement of a range of gate lengths on a single wafer. In this way the sensitivity of device performance to gate length can be conveniently explored, particularly as regards RF performance.

One of the aspects of silicon integrated circuit fabrication, which differs from the GaAs case, is the multiplicity of processing steps which are used. These steps originate with the flexible ability to form and tailor junctions and with the extensive use of complementary devices (npn and pnp MOSFETs or bipolar transistors, especially in digital circuits. This flexibility is reflected in multi-step processing schedules which can require nearly 100 individual steps to realize a given circuit. The discussion of MICROX process development begins with overviews of the process sequences used to fabricate the exploratory devices and the demonstration circuits for this program.

For this program two main processing sequences have been used: a CMOS (Complementary MOS) and an n-channel FET one. The CMOS process sequence provided both n- and p-channel FETs for exploring the geometric control of RF device behavior. A somewhat simpler n-channel device process was used to fabricate demonstration circuits. Ultimately, because of the need to handle passive components for circuit uses, and to thin the wafers and provide ground plane contact vias, this process required more than 90 steps.

3.2.1 Typical Processing for CMOS Devices

The following abbreviated summary, treats groups of steps listed in Appendix A, Table A.1 which are required to produce specific MICROX device features. This is intended to provide an appreciation for the overall MICROX device processing sequence, especially to those readers whose past experience has been with either GaAs MMIC processing or silicon processing related to digital circuits.

Background information is provided in Steps 0 through 2. Steps 3 through 6 are used to accurately thin the outer silicon layer (about 160 nm-thick initially) on selected wafers to thicknesses of 150, 130, and 100 nm, beginning with wafers. Ultimately, after all process-required oxidations, target thickness values for the active silicon in the FET gate regions were 120, 100, 80, and 50 nm, depending on the wafer.

Provisions for the DSW (Direct Step on Wafer) and global alignment marks for optical and E-beam lithography are made in steps 7 through 9. E-beam lithography is used for gate delineation (and metal reinforcement of the poly-silicon gate). Steps 10 through 20 include the channel implants for the three types of RF FETs: n channel enhancement mode, n channel depletion mode, and p channel enhancement mode. In steps 21 through 27, the individual FET islands (or mesas) are delineated and a LOCOS planarizing oxide is grown exterior to the FET mesas. A field oxide for the non-channel area of the FET mesas is produced in steps 29 through 31.

In steps 32 through 34 the field oxide is removed from the channel and immediately adjacent regions. Step 35 is a crucial one since it provides the thin gate oxide (designed to be 10 nm-thick). In steps 36 through 40 electron beam patterning of the poly-silicon gate layer is done. For this experimental effort, the electron beam exposure conditions are changed in a controlled fashion to provide a range of exposed gate lengths from 0.20 to about 1.0 micron.

Steps 44 through 51 provide moderately heavy doping (selected p- and n-type dopants for the complementary devices in this lot) of the portions of the contact regions immediately adjoining the active channels. These moderately doped regions are subsequently covered by the silicon nitride sidewalls of the gate structure (Steps 53 and 54). Finally, for the n-channel FETs, the heavily n-type source and drain contact regions which will receive metallization later were provided in steps 55 through 59.

Completion of the p-channel FET implants (Steps 60 through 63) is followed by rapid thermal annealing of all the implants (Step 64). In Steps 65 through 69 titanium silicide processing for low resistance

contacts to the devices is done. A standard forming gas anneal for surface state reduction (Step 70) is followed by a sequence (Steps 71 through 74) to provide additional gold for the gate fingers to minimize rf losses in the short, wide gate structure.

Step 75 provides the pattern for the external contact metal, which is done in two stages. In Step 76 a sequential Cr/Pd evaporation is performed *in situ*, following an ion milling step to remove residual oxide. A layer of gold is evaporated (Step 77) over the Cr/Pd base and the photoresist mask is removed (Step 78) to delineate the contact and interconnection metal. Selected devices (with two gate finger geometries) can be given preliminary testing at Step 79. The remaining steps (80 through 86) provide for thick plated airbridges to realize the large device peripheries. These are needed to deliver the current, power, and impedance levels required in microwave devices for a variety of applications. Final device testing is done at Step 87.

3.2.2 NMOS Processing for Devices and Circuits

The process sequence for MICROX circuits using NMOS FETs, given in Table A.2 of Appendix A, differs in three major respects from the CMOS processing sequence described above. First, junction formation was simpler, since only N-channel enhancement mode devices were produced. Second, the fabrication of nichrome resistors and capacitors with a silicon nitride dielectric were required to implement the demonstration circuits. Finally, since the demonstration circuits required microstrip interconnections, the wafers were thinned to 100 μm, vias were formed, and backplane metallization was provided. The net effect of these changes was a somewhat longer processing sequence than for the CMOS FET case.

The purpose of this description is to relate the simpler NMOS processing sequence to the CMOS fabrication sequence, which was given in the preceding section. There was no thinning of the silicon overlayer on this group of MICROX wafers. As supplied the wafers had a silicon layer of 1600 A nominal thickness on a buried oxide of 3800 A thickness. Steps 5 through 8 produce starting alignment marks for electron beam lithography; steps 9 through 12, for optical lithography. In the earlier CMOS processing case, the marks were all prepared in steps 7 through 9, using E-beam methods, making subsequent alignment of optical patterns more difficult.

In steps 13 through 21, the processing is done to produce as nearly planar a surface as possible. This is particularly important in the case of the demonstration circuits, to reduce the risk of open interconnecting lines between the oxide-isolated active devices. Because of this requirement, a more detailed description of the planarization process is given below in Section 4.2.2.

Steps 22, 23, and 24 in the fabrication of the n-channel FETs correspond to steps 31, 18, and 20, respectively, in the CMOS description of Table A.1 in Appendix A. The apparent change in sequence is an artifact of the more complex device processing sequence which is required to produce both p- and n-channel devices in the complementary case.

The remaining processing follows the sequence of the complementary devices, with simplifications due to the elimination of p-channel enhancement mode FETs and n-channel depletion mode FETs. Additional streamlining of the process is due to the use of implants alone for gate doping, rather than including steps to evaluate diffused doping of the gates. Steps 25 (DSW exposure of the active area mask) through 35 (LDD arsenic ion implant) generally correspond to Steps 32 through 46 in the CMOS sequence. Steps 36 (nitride deposition for the gate sidewall) through 50 (rejection of gate metal reinforcement) relate to steps 53 through 74 in Table A.1. Nichrome resistor fabrication (Steps 51 - 53) has no correspondence in the CMOS FET fabrication description. The contact and interconnection processing of Steps 55 through 58 corresponds to Steps 75 - 78 in Table A.1. Capacitor processing in Steps 59 - 62 is also unique to the circuit fabrication. Completion of front-side processing in Steps 63 (post mask for airbridges) through 86 (stripping of the post resist) corresponds to Steps 80 through 86 in the CMOS sequence.

After a check of RF test transistors (Step 69), steps 70 through 91 provide for wafer thinning, via formation, backplane metallization, and separation of the wafer from its support.

3.3 Circuit Designs

3.3.1 Background

The design plan for devices and circuits on this program drew on prior experience with GaAs FET technology and applications. As described in Section 3.1, the MICROX FET designs provided a variety of device geometries with a range of channel lengths (achieved by direct E-beam delineation of the gate) for different total width configurations referred to as structure types. These structure types used parallel combinations of basic source-gate-drain elements with individual element widths of 20, 30, 50 and 100 μm to realize overall gate widths from 40 to 2,000 μm.

As shown for a typical example in Figure 7, the measured device characteristics over a wide frequency range were fitted to a modified GaAs FET small signal equivalent circuit model with 15 parameters. The figure shows measured and fitted S-parameters as well as the measured and modeled MAG/MSG characteristics of the device.

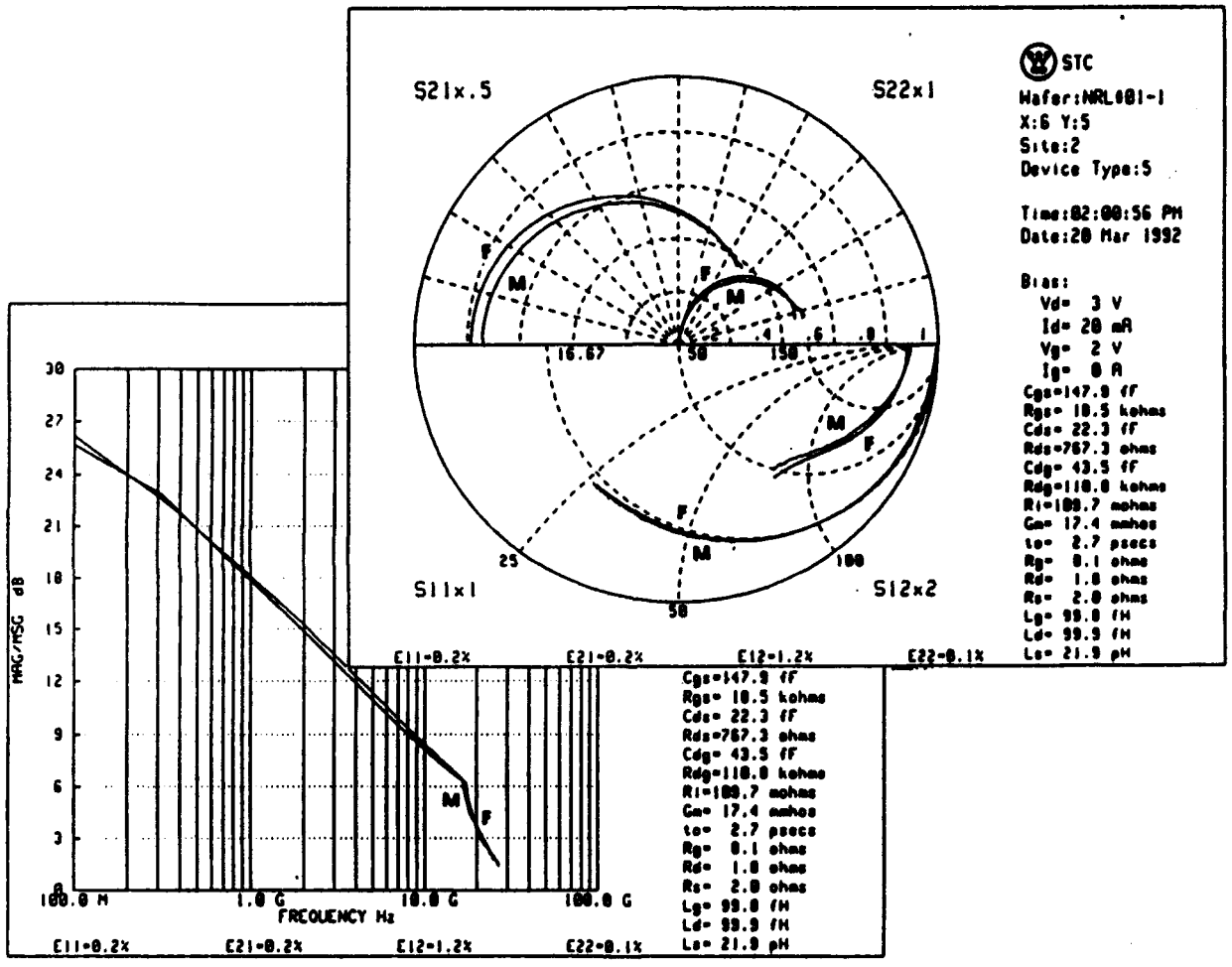


Figure 7. Example of measured (M) and fitted (F) S-parameter results, and equivalent circuit parameters, for a MICROX FET with a 380 nm-long (as written), 6 x 20 μm gate. The associated current gain behavior is shown to the lower left.

The scaling of parameters with width, illustrated in Figures 8 through 10, was used to derive a simple device model for the use in the various amplifier and mixer circuit designs.

A similar process, but with simpler models of the FET in both conducting (ON) and non-conducting (OFF) states was used to provide design information for attenuators.

3.3.2 Distributed Amplifier

The design of the distributed amplifier was based on earlier work in GaAs. It takes advantage of the circuit topology to provide a distributed transmission line with very wide bandwidth, in this case 1 to 10 GHz, between the amplifying elements. This bandwidth is achieved by incorporating the FET capacitance with inductors to produce a lumped element transmission line. As the signal propagates along the line, it appears at the gate terminals of each FET in sequence, and has an associated output voltage which is imposed on the output line. If the electrical lengths of the paths from the amplifier input through each of the transistors to the output are equal, the output signals will constructively combine. In this particular design, a coscode pair is utilized for amplification. Lumped inductors in both the input and the output lines are used to provide the distributed transmission lines for the circuit.

Figure 11 summarizes the parameters of the equivalent circuit of the MICROX FET, derived from measurements, which was used in designing the distributed amplifier, illustrated schematically in Figure 12, and as a chip layout in Figure 13. Several iterations of the design values were made before the modeled performance shown in Figure 14 was obtained.

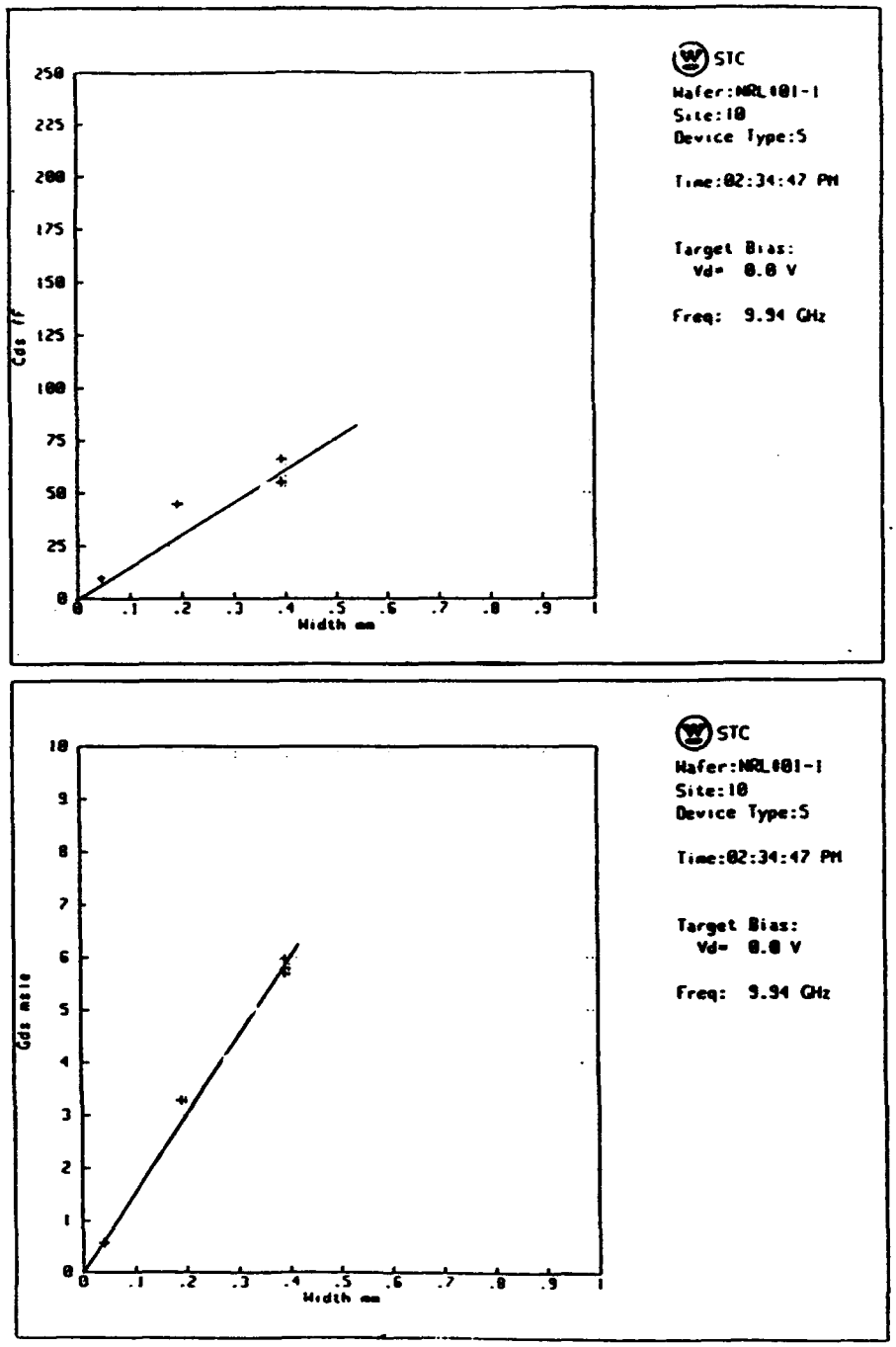


Figure 8. Influence of width scaling on the drain-to-source capacitance (top) and output conductance (bottom) of MICROX FETs with 278 nm-channel length.

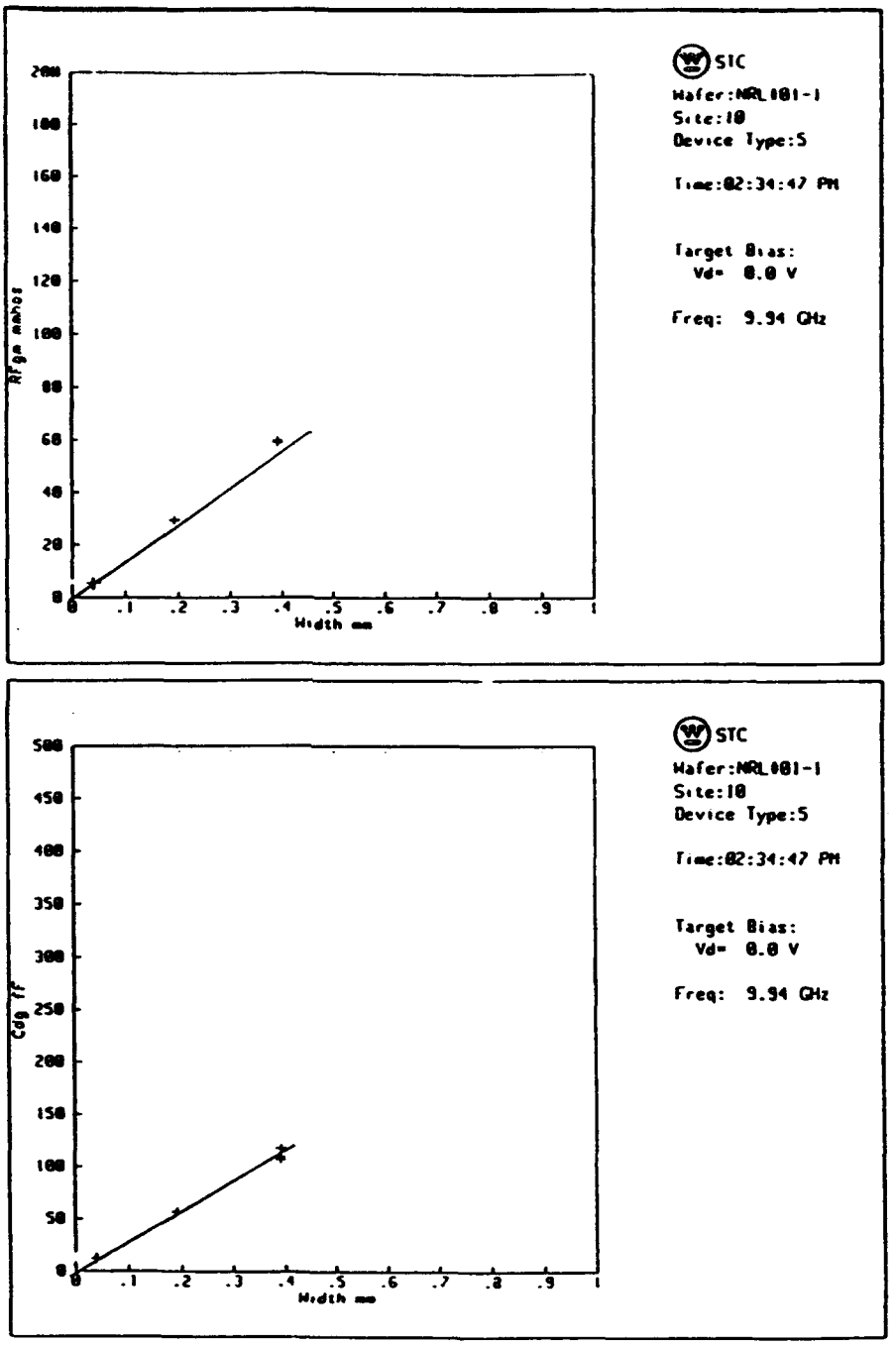


Figure 9. Width scaling influence on the RF transconductance (top) and the drain-to-gate capacitance (bottom) of MICROX FETs with 278 nm-channel length.

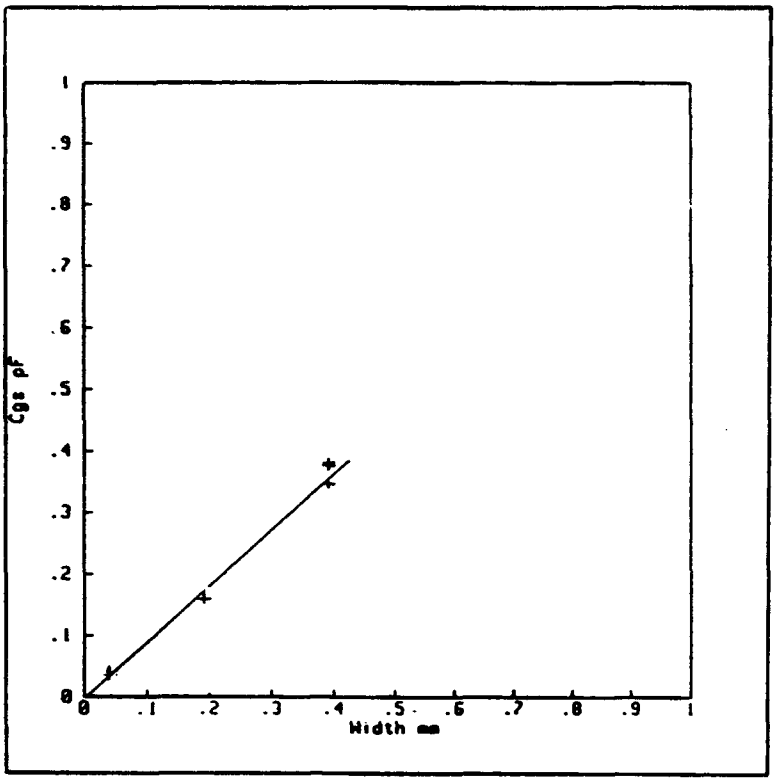


Figure 10. Gate-to-source capacitance scaling with width for MICROX FETs with 278 nm-channel length, corresponding to Figures 9 and 10.

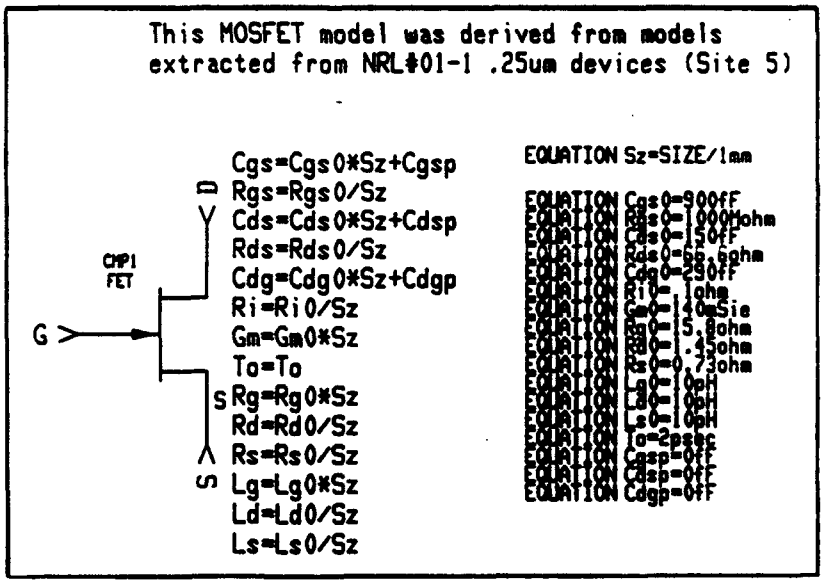


Figure 11. Model used for MICROX FETs, derived from measurements on devices with a drawn gate length of 279 nm. The values given are for a gate periphery of 1 mm.

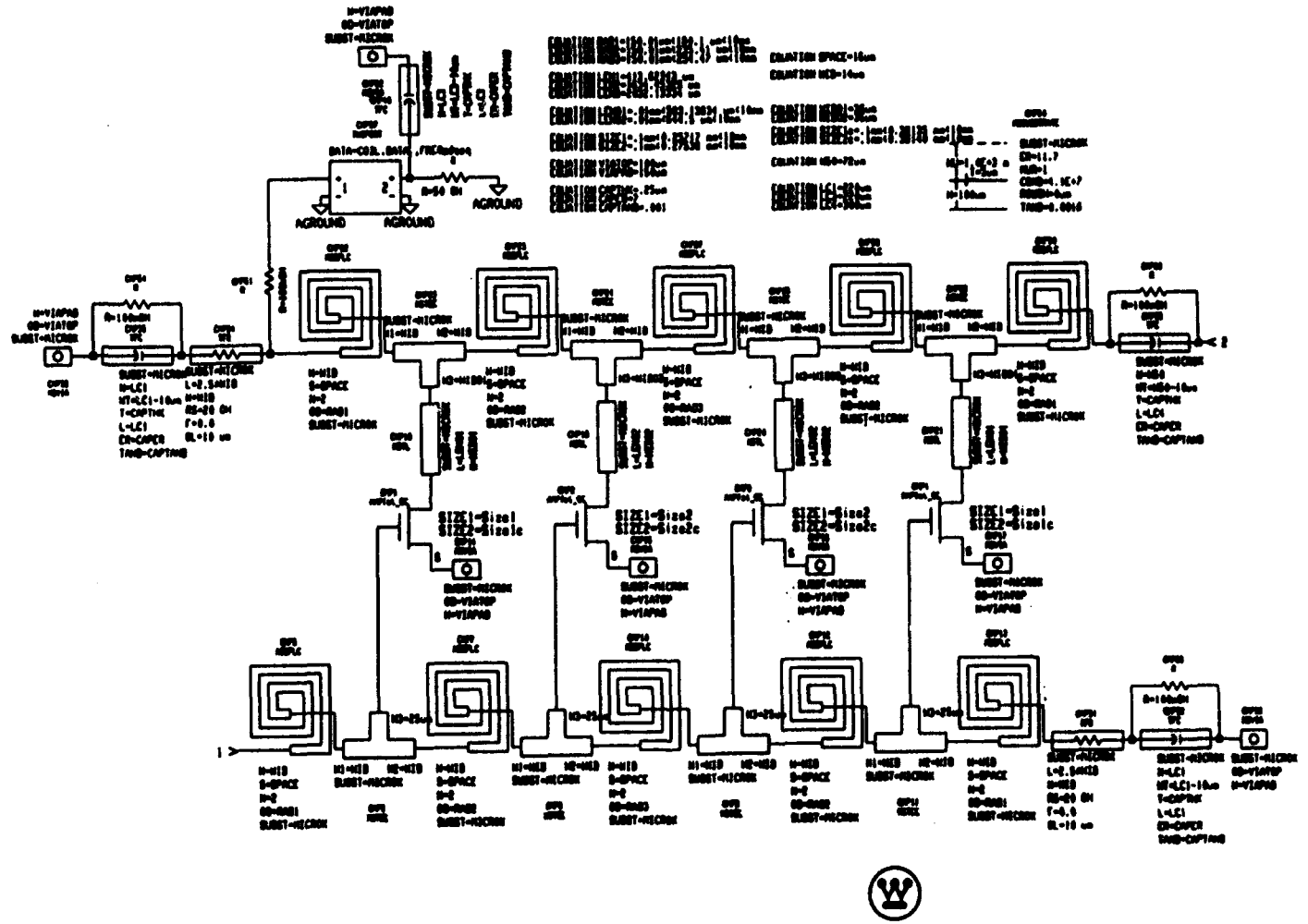


Figure 12. Circuit schematic diagram for a DC to 10 GHz distributed amplifier using MICROX.

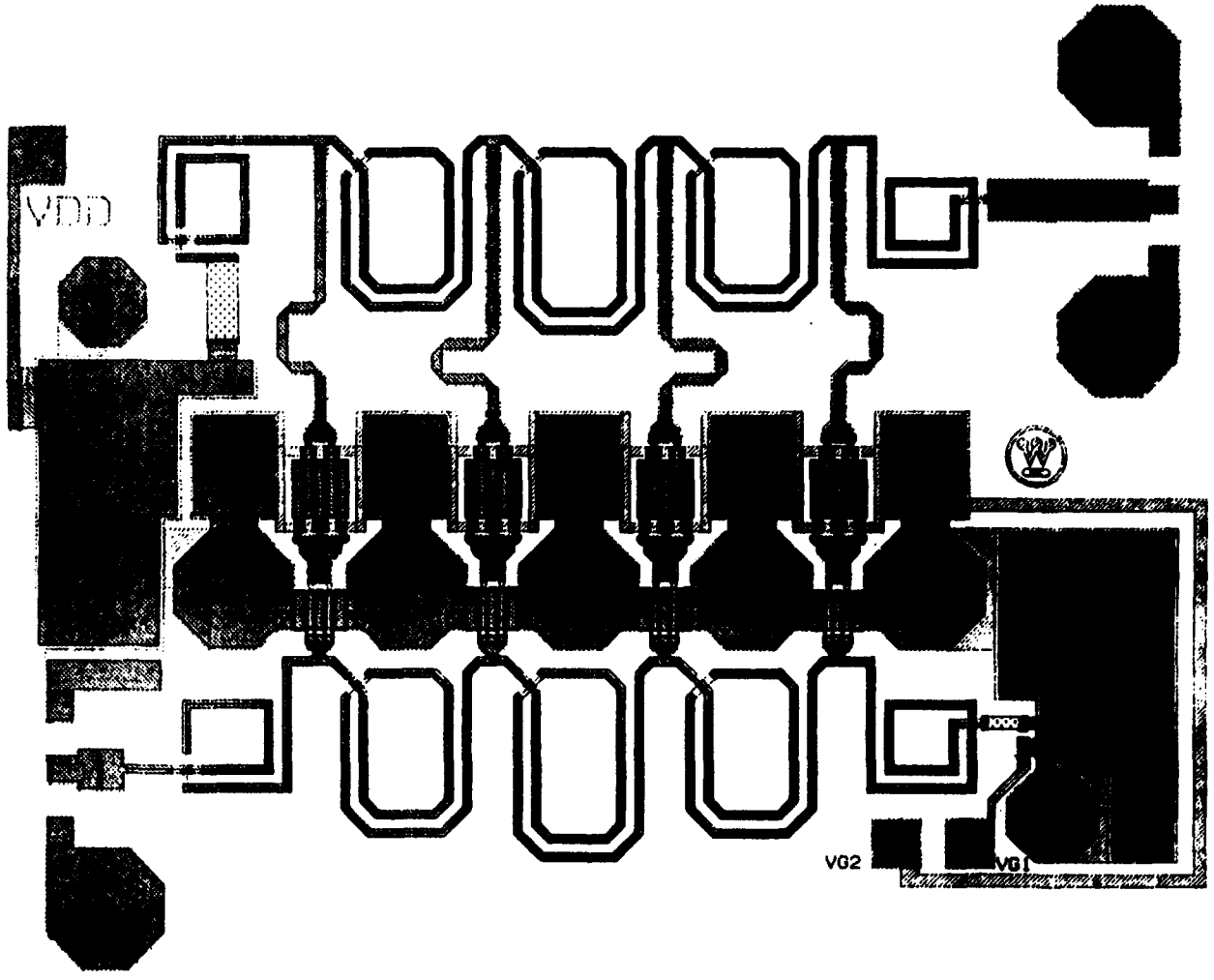
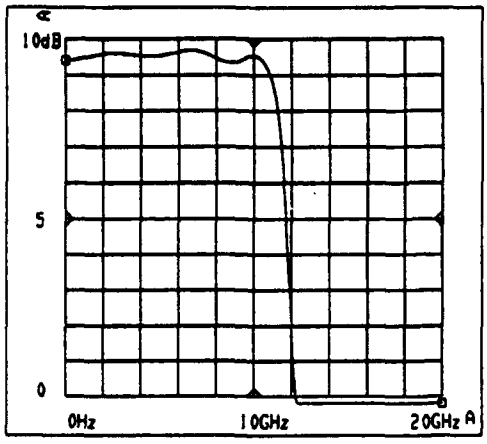
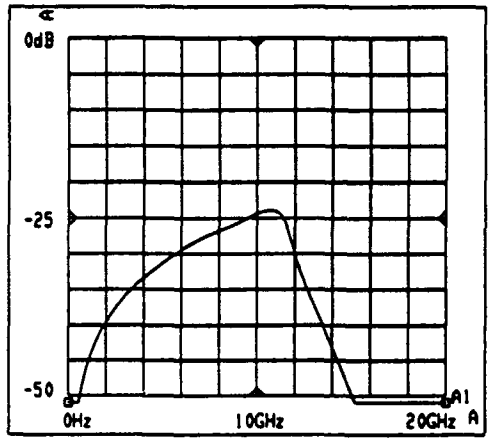


Figure 13. Integrated circuit mask layout for the DC to 10 GHz MICROX distributed amplifier.

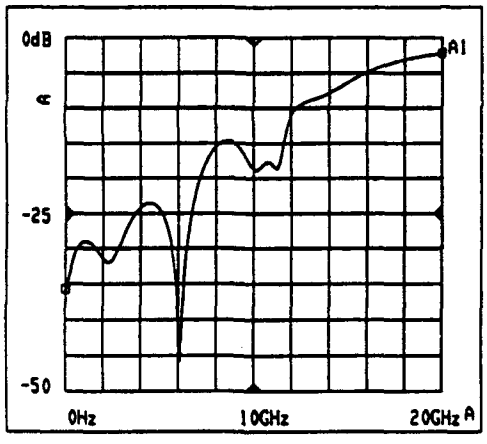
GAIN



ISOLATION



INPUT MATCH



OUTPUT MATCH

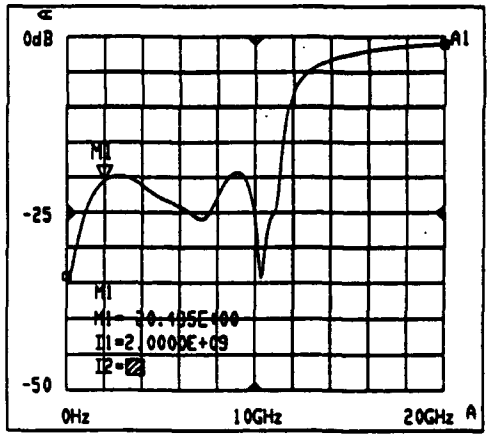


Figure 14. Simulated response of the MICROX distributed amplifier.

3.3.3 Multi-stage Amplifiers

Two L-band amplifiers provide the opportunity for comparing the performance of circuits using conventional passive elements (spiral inductors in the 2-stage amplifier of Figure 15) with those using space-saving, active device-based inductors in the 3-stage circuit (Figure 16). The high Q of the spiral inductors fabricated on the MICROX substrate is at the heart of the two-stage amplifier design. For the three-stage amplifier, the small FET structure which is used allows biasing into the conducting state. The added gate-to-source capacitor (Figure 17) provides an RF short which holds the drain-to-source voltage constant, acts as a high frequency choke, and extends the low frequency capability of this circuit (Figure 18).

3.3.4 Broad Band Mixer

A mixer implemented with FETs was chosen for this circuit, particularly because the double balance mixer provides for a natural reduction of odd mixing products. A diagram of the core mixer circuit is shown in Figure 19, with the predicted conversion gain characteristic shown in Figure 20. Figure 21 shows the high bandwidth to be expected from modelling the common mode rejection and gain characteristics of the RF and local oscillator balun. The IF balun uses a broadband operational amplifier whose gain and error characteristics tolerate capacitive loading to provide performance to 1 GHz (Figure 22). Overall, this MICROX MMIC design (Figure 23, top) offers 10:1 bandwidth with 5 dB of conversion gain (Figure 23, bottom).

3.3.5 Digital Attenuator

The low parasitics associated with MICROX devices allow compact, lumped designs attenuator circuits to be realized. Figure 24 shows designs for 1-, 2-, 4-, and 8-dB attenuator bits in MICROX. Arrangements of Π, T, or Bridge circuits are selected on the basis of the critical resistance values required for the application. The compactness of the 4-bit attenuator design is evident in Figure 25. This circuit design requires an area of only 0.8 mm x 1.5 mm. The predicted performance of the attenuator is given in Figure 26. Many systems could benefit from the availability of MICROX attenuator circuits of this type because of the high degree of integration and the lower cost, compared to GaAs parts.

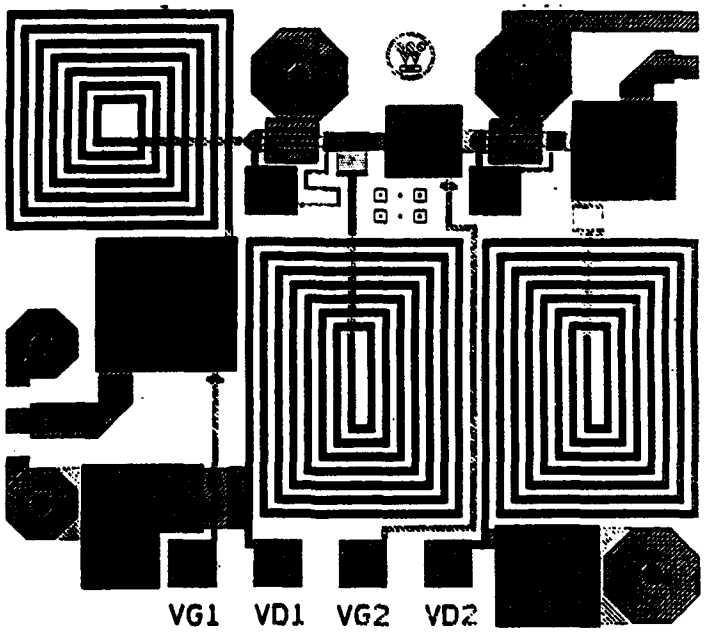


Figure 15. Integrated circuit mask layout for a 2 stage L-band amplifier in MICROX using high Q planar chokes.

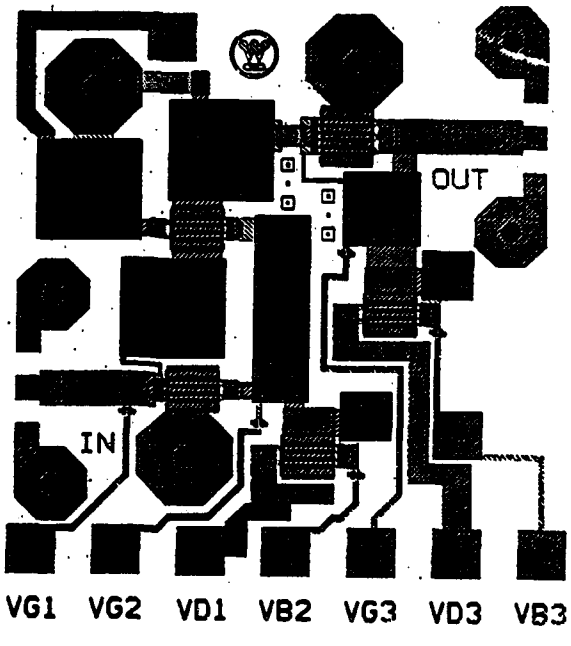


Figure 16. Compact integrated circuit mask layout for a 3 stage L-band amplifier incorporating an active choke.

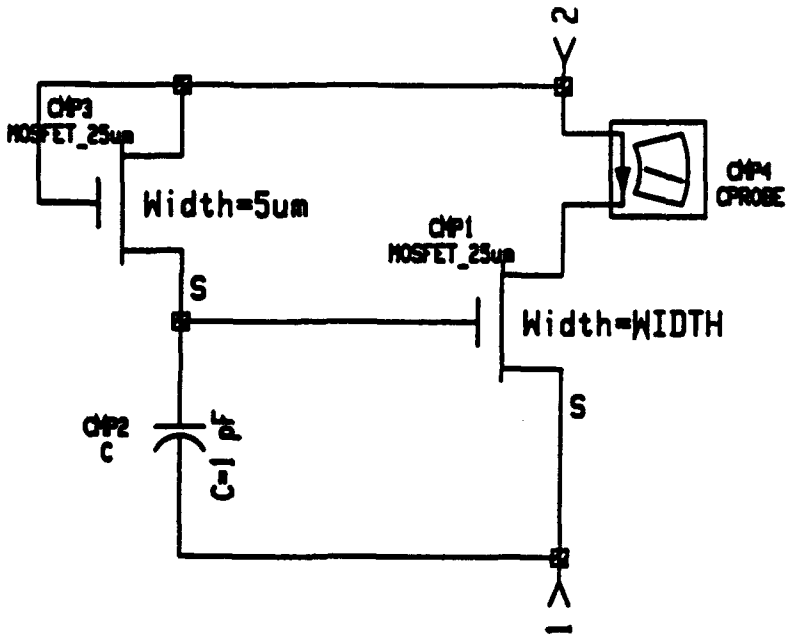


Figure 17. A small FET (upper left) biases the active FET into conduction, while the capacitance shorts its gate to RF, and keeps its drain-to-source voltage constant, providing an active choke for use in an amplifier circuit.

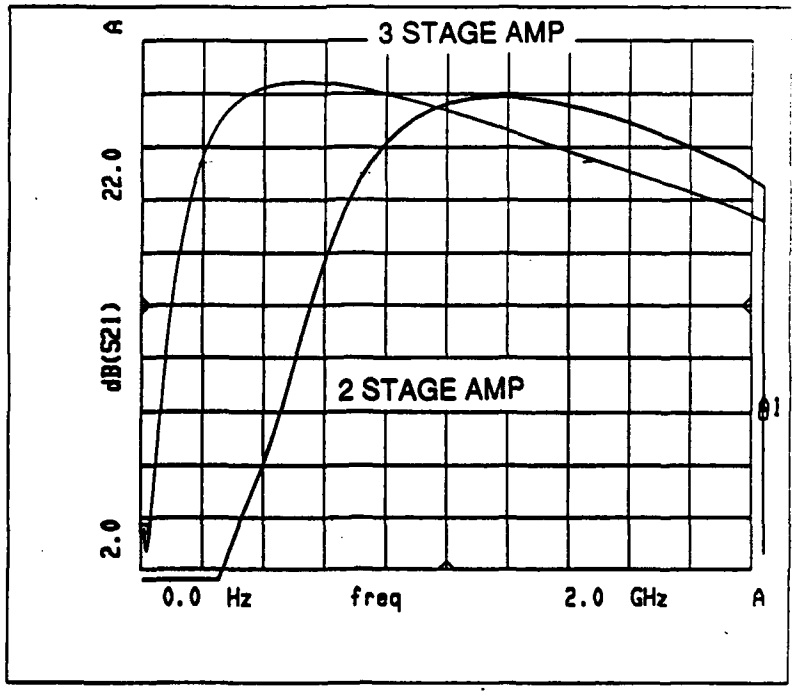


Figure 18. Simulated gain performance of the 2- and 3-stage MICROX amplifier circuits.

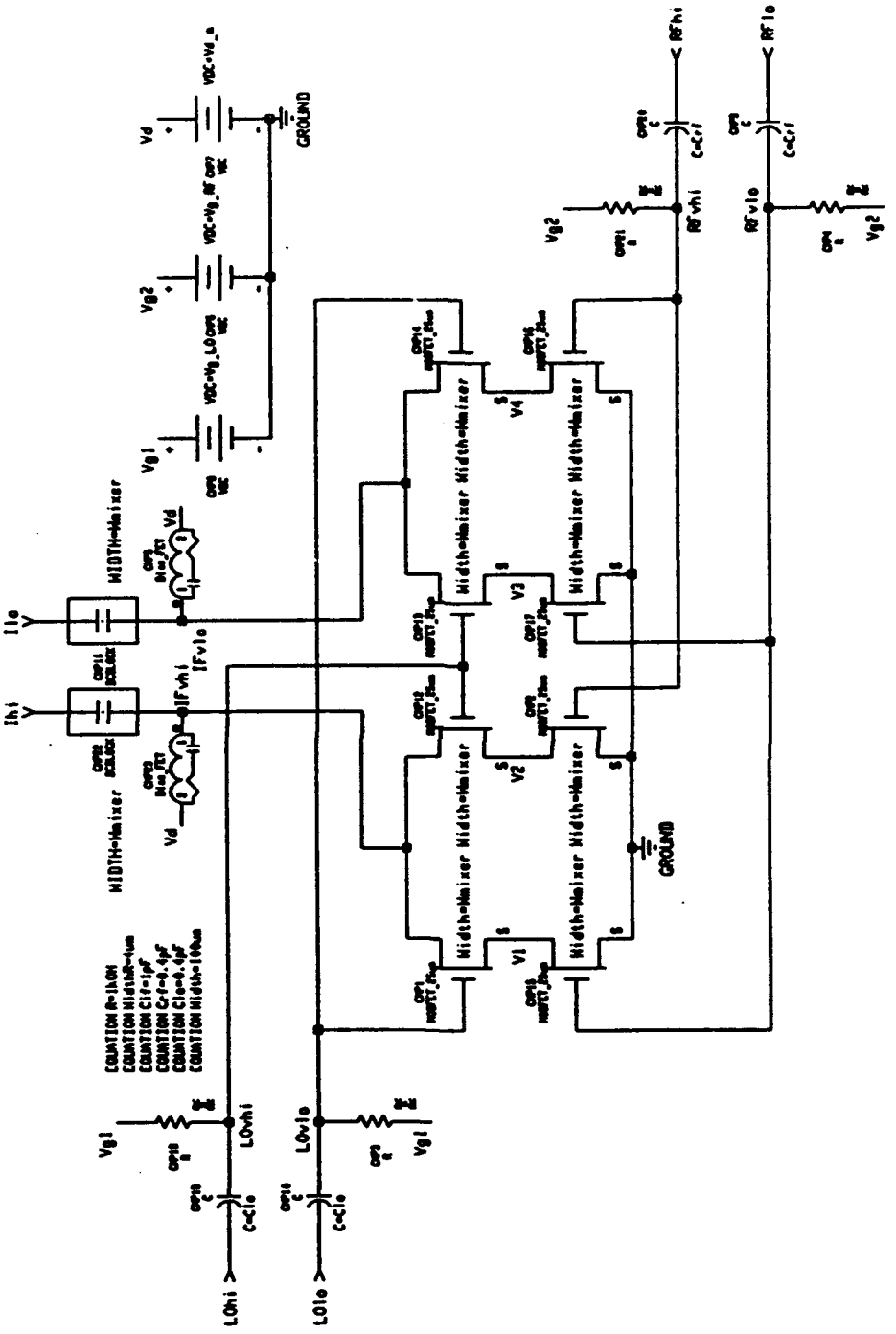


Figure 19. Diagram of the Double Balance Mixer using MICROX FETs which provides inherent reduction of the odd mixing products.

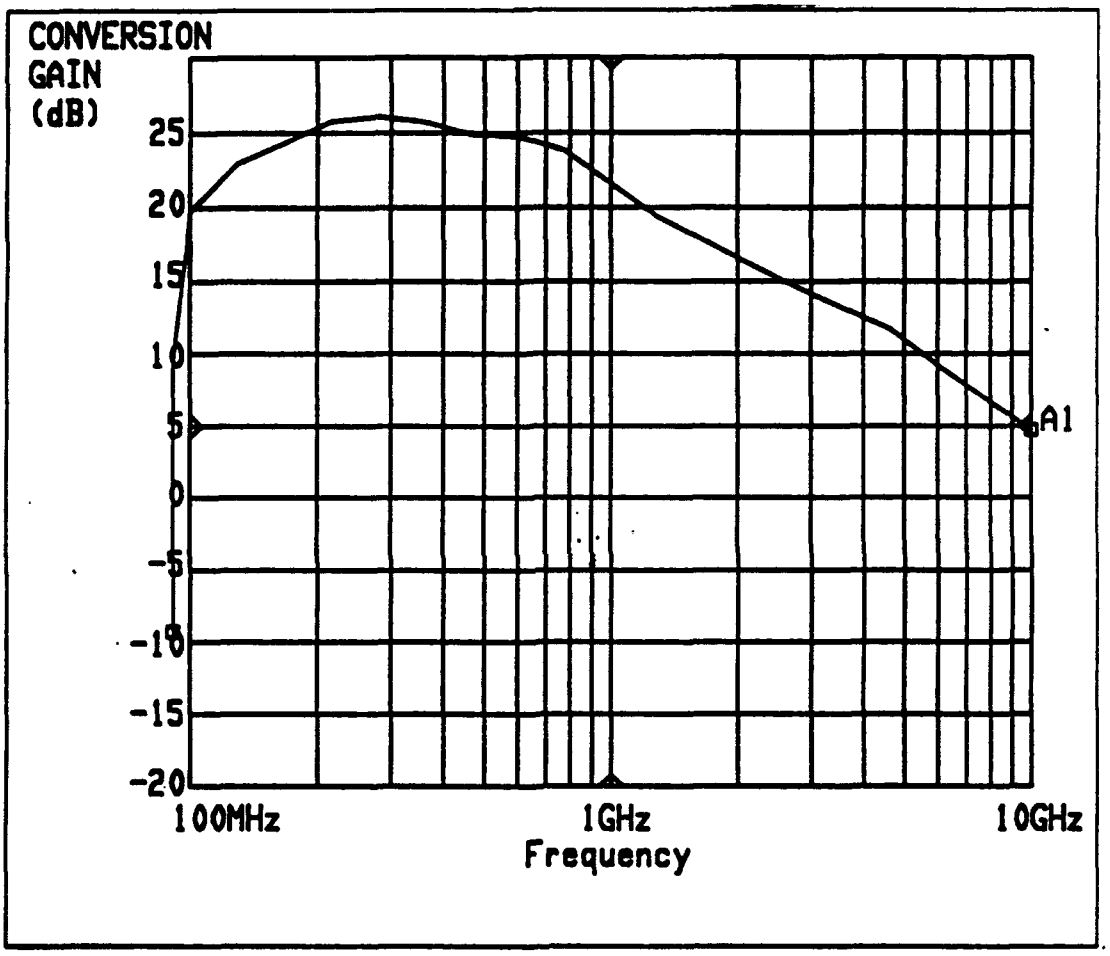


Figure 20. Conversion gain result for simulated operation of the core mixer.

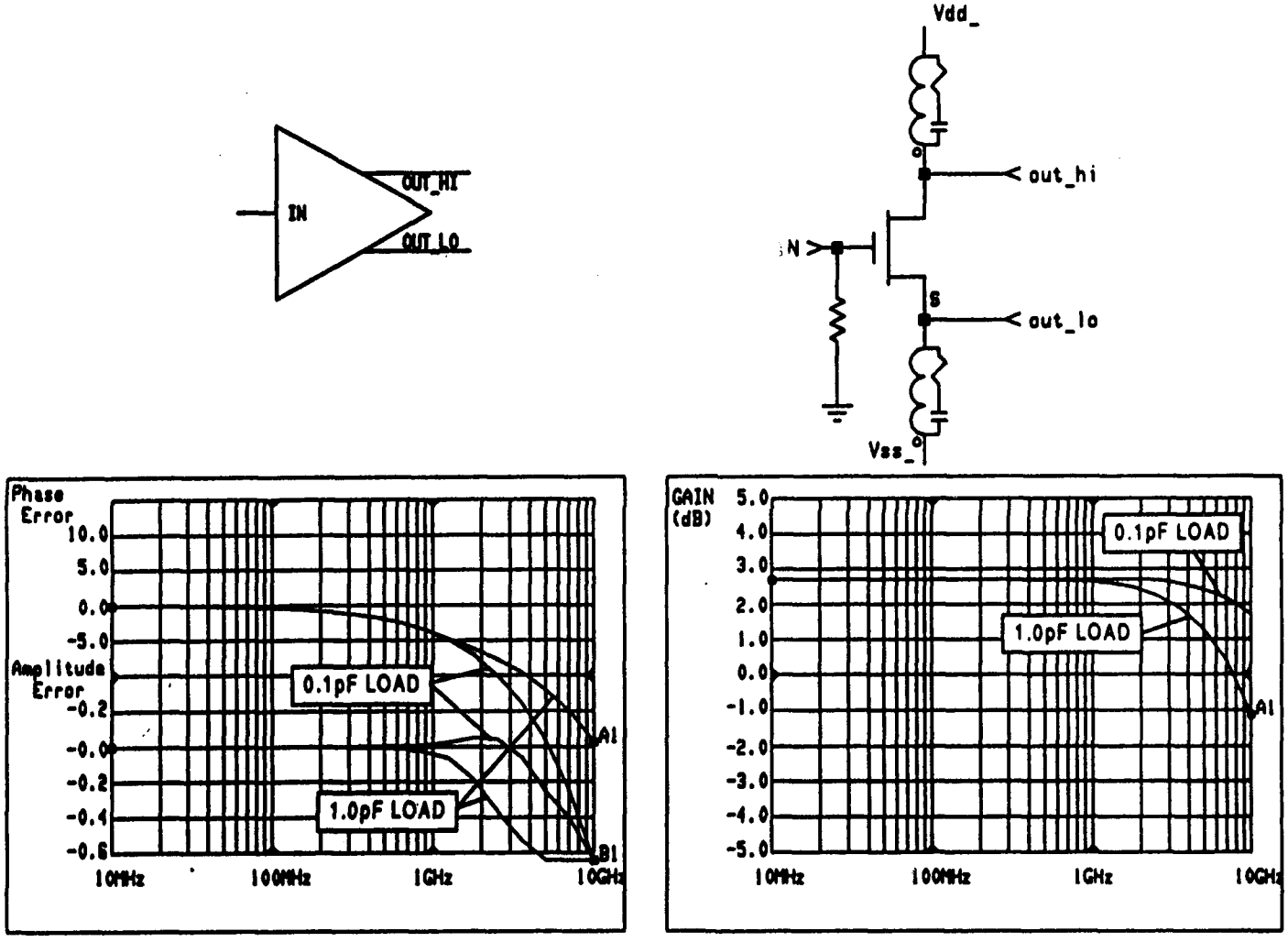


Figure 21. The RF and LO MICROX Balun has high bandwidth as shown by the simulated performance.

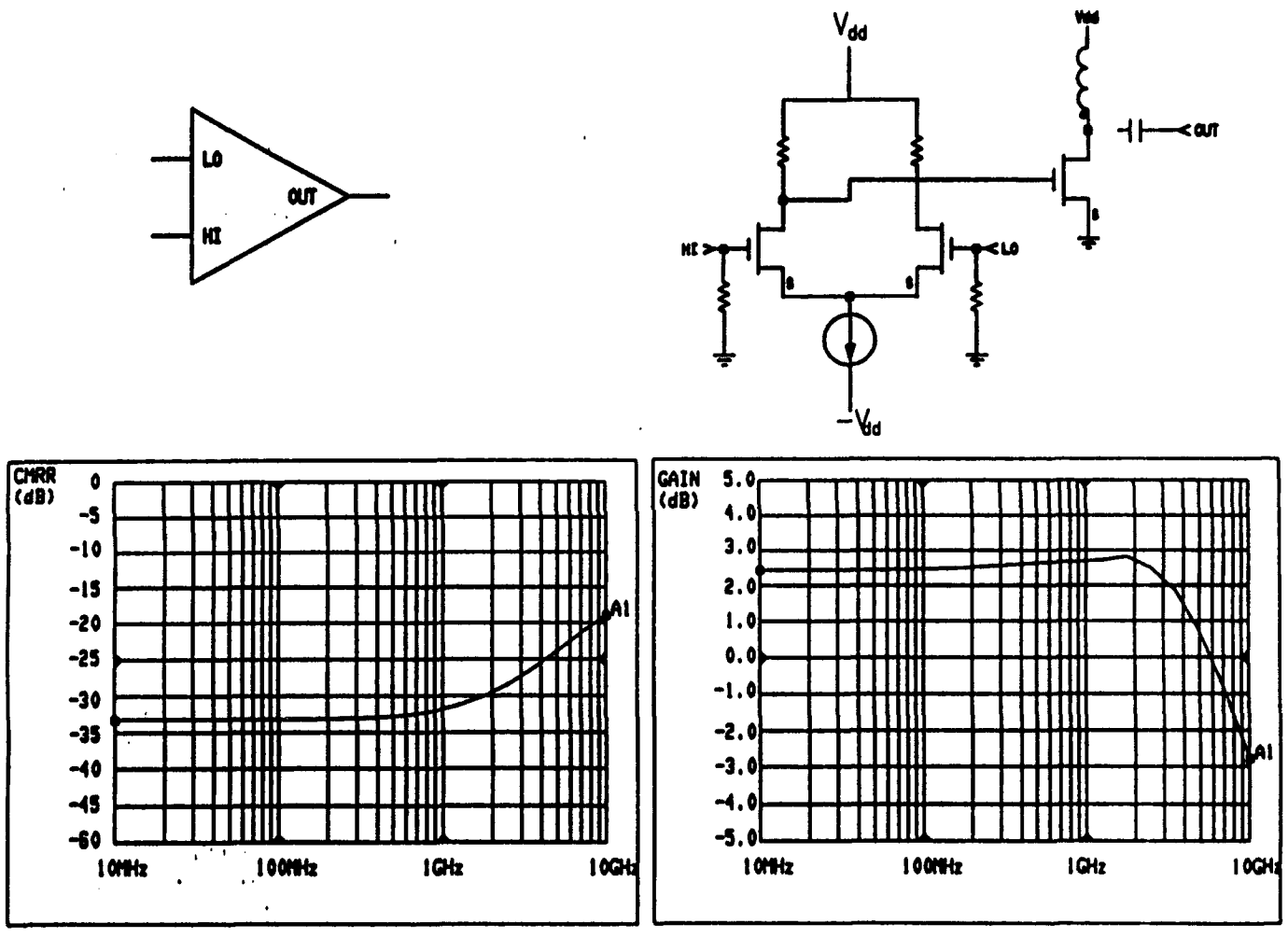


Figure 22. A MICROX broadband operational amplifier implements the IF Balun, whose simulated performance is shown here.

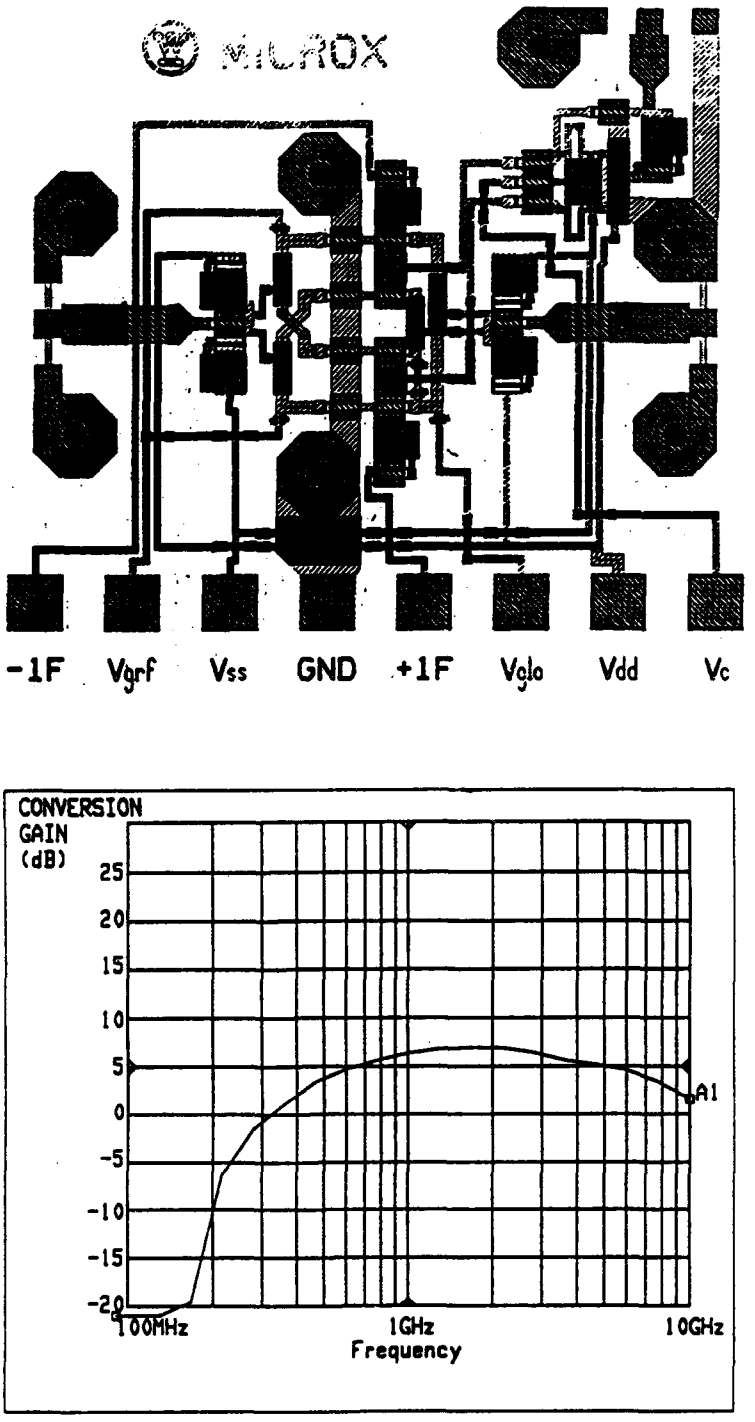


Figure 23. The MICROX mixer circuit has a compact layout (top) and a simulated response (bottom) which provides 10:1 bandwidth with 5 dB conversion gain.

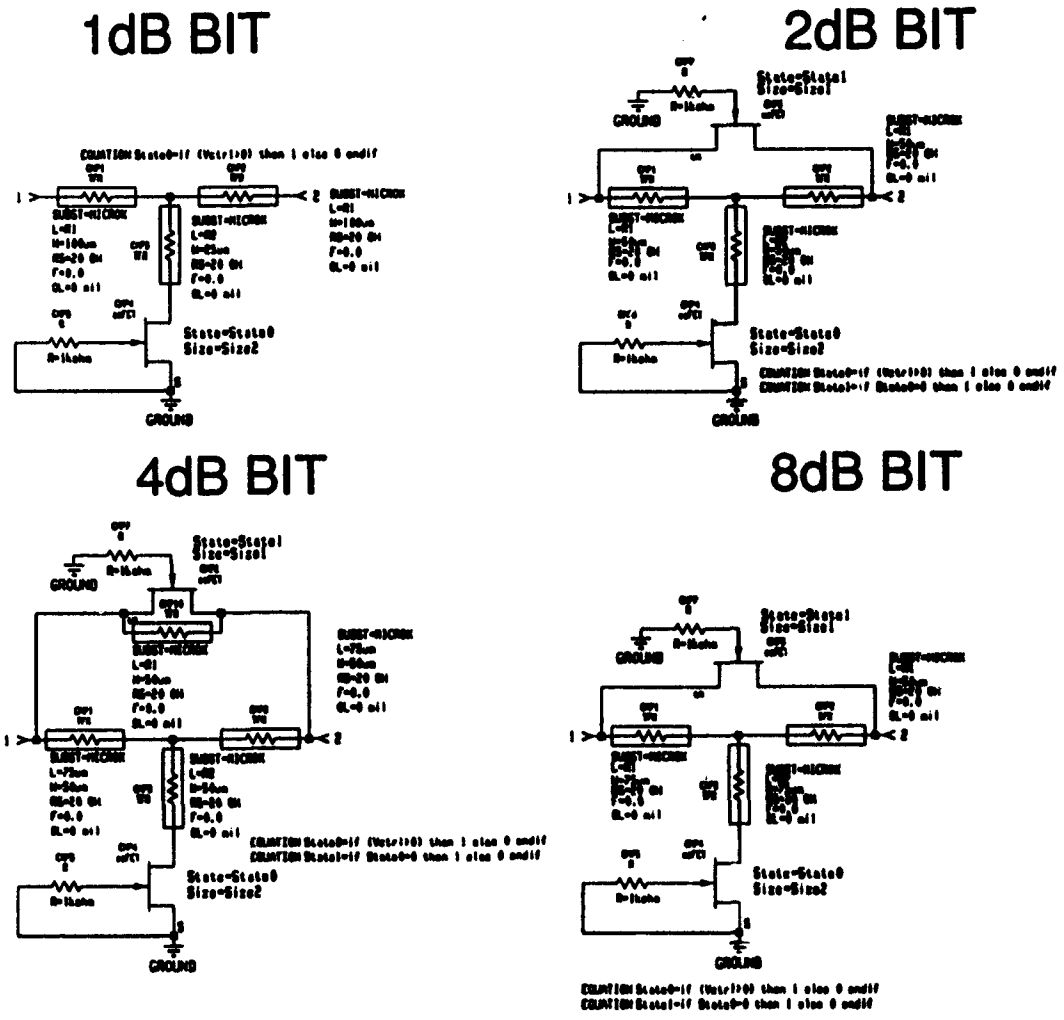


Figure 24. MICROX FET characteristics allow a flexible approach with Π, T or bridge circuits to accommodate various attenuator needs.

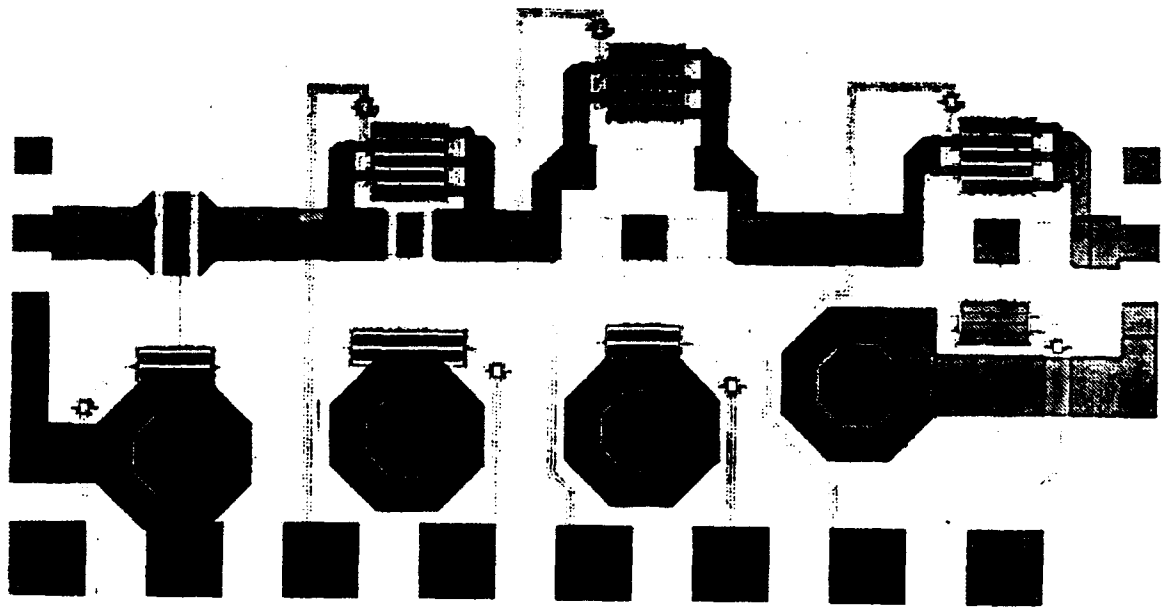


Figure 25. Compact circuit mask layout for a 4-bit, L/S-band digital attenuator using MICROX.

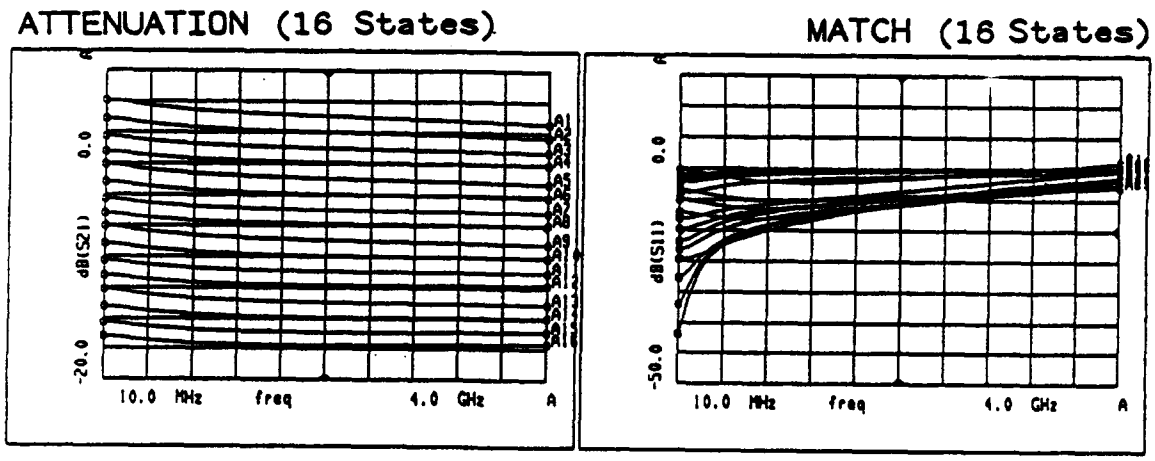


Figure 26. Predicted broadband performance of a 4-Bit digital attenuator using MICROX.

4. TECHNICAL RESULTS

The purpose of this section is to relate the practical results of the program, and to describe the major problems which were encountered and resolved.

4.1 FET Performance

A major aim of this program has been to fabricate and evaluate in MICROX silicon, which uses a high resistivity substrate with the added advantages and capabilities of a silicon-on-insulator (SOI) structure, MOSFETs that are designed for operation at frequencies above 1 GHz. The main feature of these designs is the ability to use large peripheries to provide devices with impedance and current-handling capabilities required in microwave circuit applications. Generally, the past interest in MOSFET speed issues has been on small devices intended for use in fast logic circuits. The work on this program explores the potential for devices with much larger peripheries than those in conventional logic and memory circuits. The results in the following sections cover topics ranging from I-V behavior of devices with agresssive geometries to the first demonstration of significant microwave power from silicon MOSFETs.

4.1.1 DC Characteristics

Device performance characterization was possible only after the major part of device processing was complete to provide adequate metal contacts to the active regions of the FETs. Figures 27 and 28 give examples of typical MICROX FET behavior for N-channel FETs. These devices were measured at an intermediate stage of processing, before airbridging made available empirical devices with more than two gate segments. Both of the devices treated here have similar transconductance values - 125 to 127 mS/mm - but the details of their structure are different. The simpler device (Figure 27) has no low doped drain (LDD) and an effective gate length of 0.55 μm. In the case of the LDD device, the competing effects on current capability of a shorter gate length (0.24 μm) and the additional resistance due to the lower doping in part of the drain region result in a comparable value of transconductance. Drain current enhancement (by about 25%) due to reducing the gate length from 0.55 μm to 0.25 μm, even with the higher drain resistance of the LDD structure, is evident in Figure 29. A major benefit of drain structure engineering with the LDD is the increase in drain voltage capability of these devices to the 5 volt range (Figure 30).

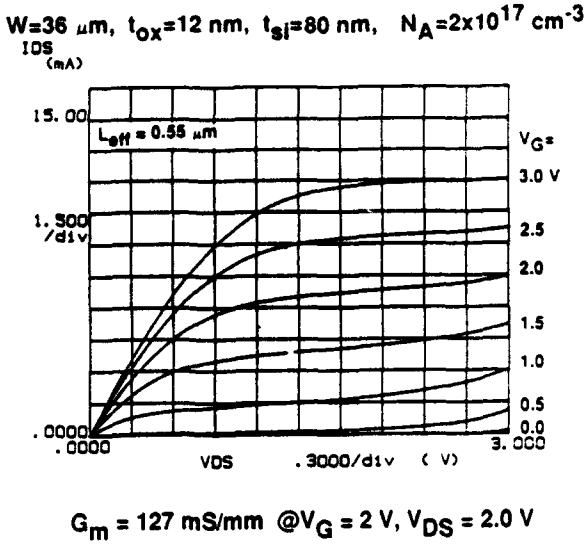


Figure 27. High transconductance behavior for a typical grounded source n-channel MICROX FET (no LDD) with an effective gate length of 0.55 μm.

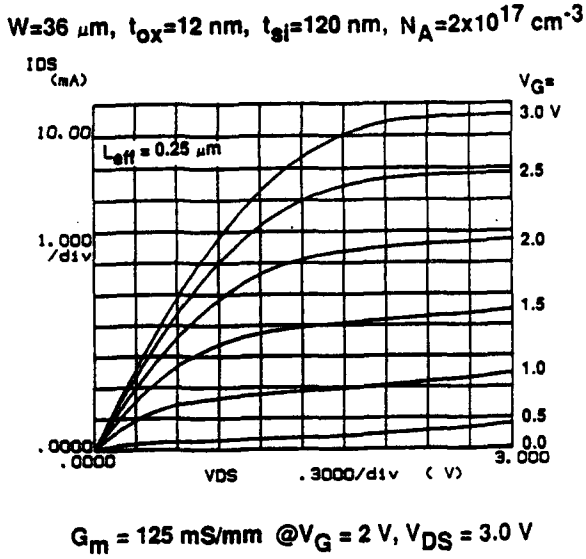


Figure 28. An n-channel MICROX FET with an LDD and 0.24 μm effective gate length provides 125 mS/mm of transconductance.

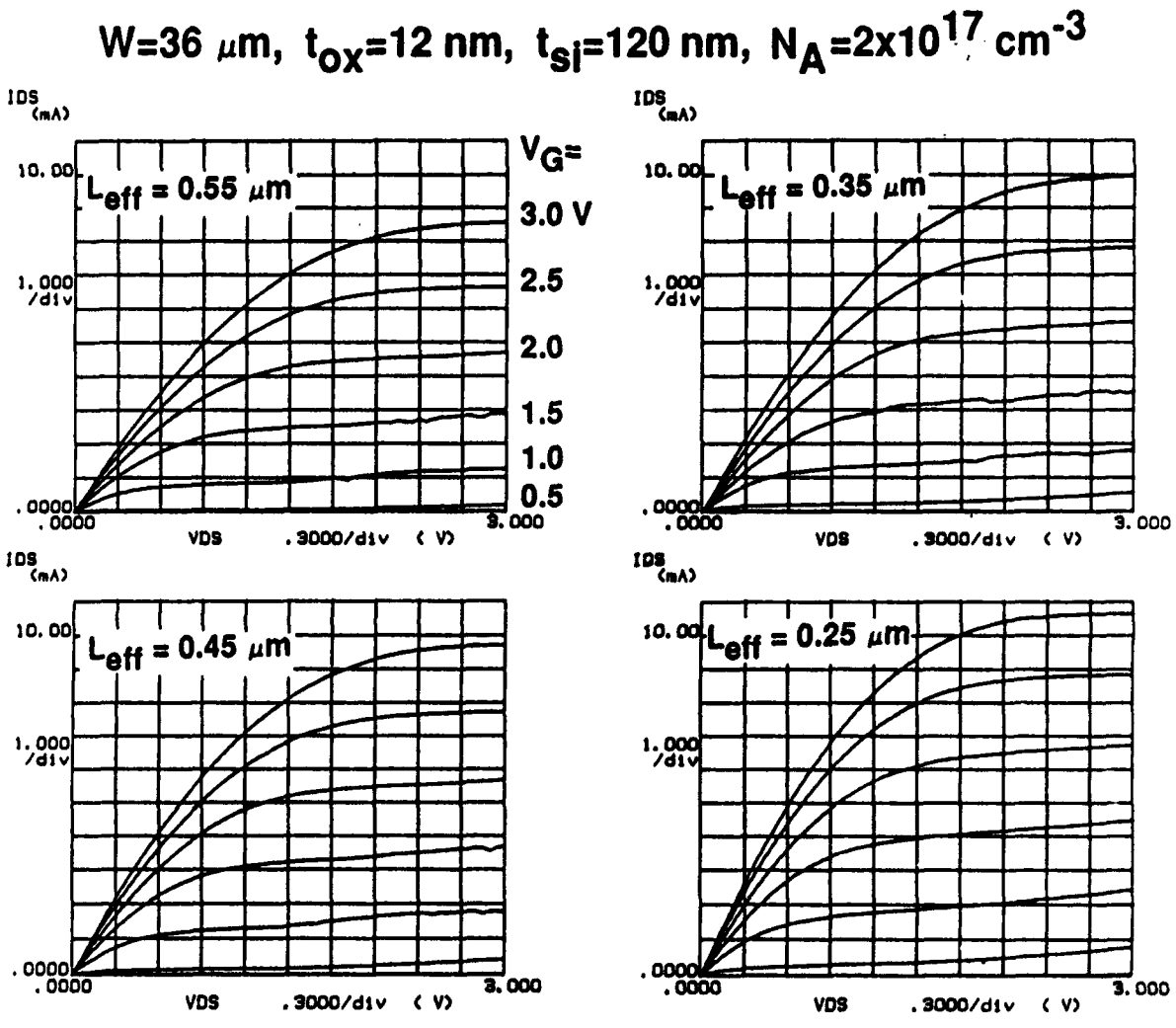


Figure 29. N-channel FETs with LDD structures show benefits in increased transconductance as the gate length is reduced to 0.25 μm.

The exploration of structural and design benefits on the capabilities of n-channel FETs was of most concern in this program. These devices are expected to be the most widely used in RF applications. There was additional interest in the performance of p-channel FETs whose co-fabrication was accomplished using the process sequence described in Table A.1 of Appendix A. P-channel FETs are particularly significant since they are not practically available in GaAs due to its low hole mobility. As seen in Figure 31, p-channel MICROX FETs have a maximum transconductance only about a factor of 2 below that of comparable n-channel devices (upper right, Figure 29). This result, in combination with the RF performance for p-channel FETs described in the next section, indicates good prospects for future development of MICROX circuits based on complementary RF devices.

4.1.2 Frequency and Power Capability

Figure 32 shows measured MAG/MSG results for a MICROX FET with a 4 x 50 micron-wide gate structure and a 279 nm measured gate length. In this case, the extrapolated value of f_{max} is 32 GHz. For comparison, a P-channel FET (with measured gate length of 402 nm and the same 4 x 50 micron gate structure) gave an f_{max} value of 20 GHz, as shown in Figure 33. The ability to obtain complementary MOSFET performance of this type is important for efficient RF circuit applications of the MICROX approach.

S-parameter measurements were made for all grounded source n-channel FETs devices on this wafer with a 4 x 100 micron-wide gate geometry. Figure 34 shows maximum available gain at 9.95 GHz as a function of location for three rows of devices, including the center of the wafer. The locations are numbered sequentially, with the bottom row including numbers 1 through 8, and the top row including numbers 25 through 32. Not all locations (such as 1, 2, 7, 8, 24, 25, 31, and 32) had devices. Devices with negative values of MAG/MSG were arbitrarily assigned values of -1 dB for purposes of automated plotting of the results.

From the data shown in the upper panel of Figure 34, we can see that device performance generally improved along each row toward the right side of the wafer. This probably reflects gradients in the thickness of the top silicon layer due to details of the oxygen implantation process used to form the MICROX structure. The lower panel in this figure gives results which were obtained on the same devices before airbridging of the source regions. One consequence of the preliminary test was that only two of the four channel segments in each device could be contacted at that stage. As a result, shorter gate lengths appeared to offer no benefit in device performance.

The main effect of airbridging, as expected, was to provide more gain in all devices by adding the contribution from the two segments of

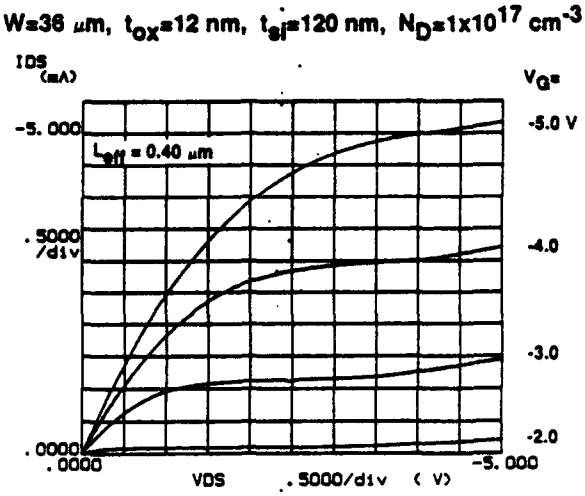


Figure 30. A large periphery n-channel MICROX FET exhibits 5-volt drain voltage capability, a benefit of the Low Doped Drain structure.

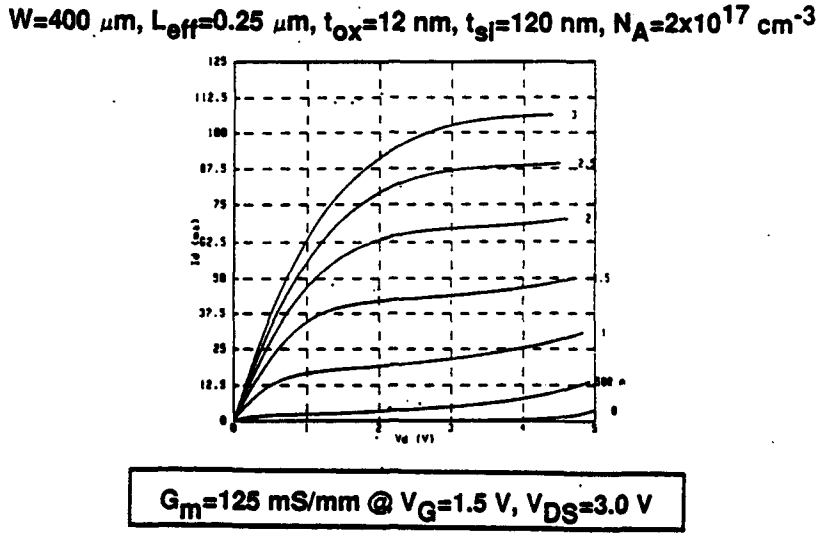
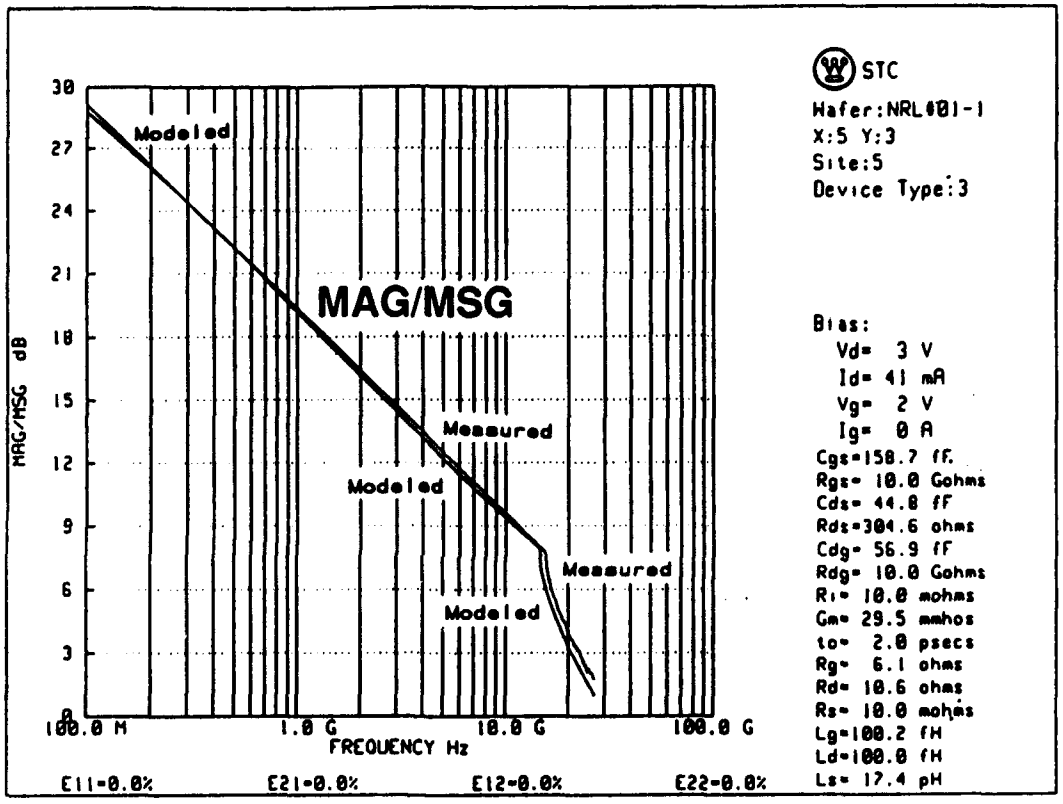


Figure 31. MICROX makes available p-channel FETs by complementary MOS processing to support high performance circuits (50 mS/mm) with reduced power dissipation.

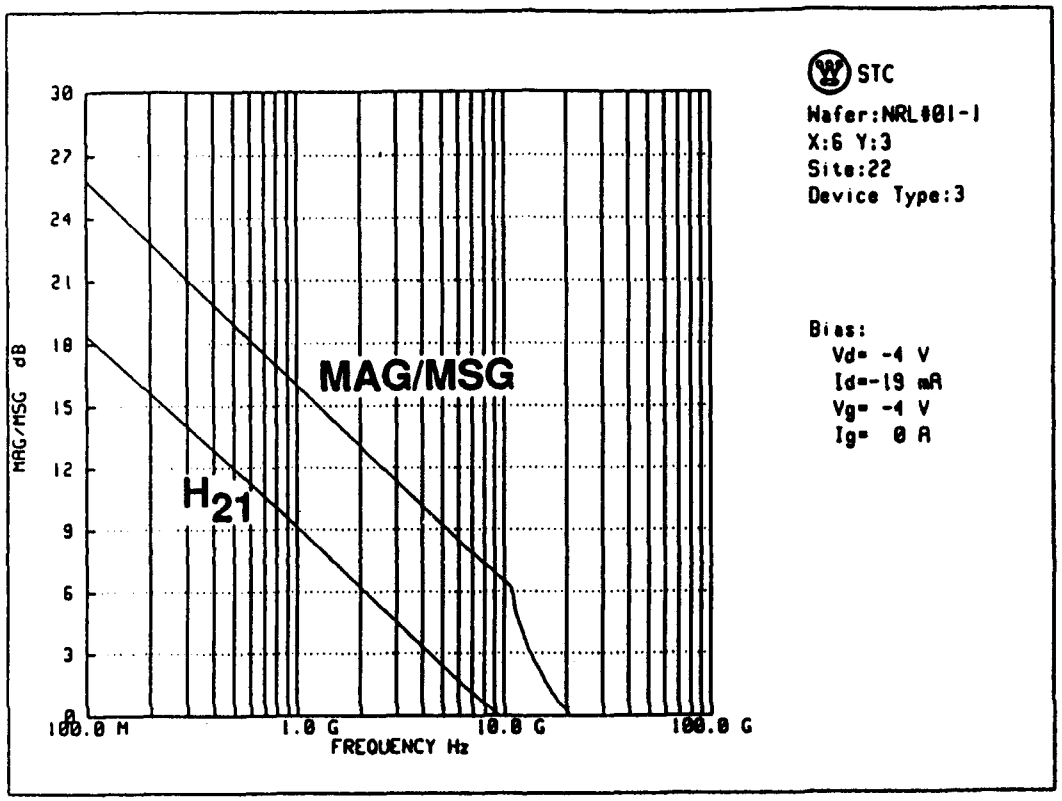


$F_t = 23.6$ GHz, $F_{max} = 32$ GHz

($L_{eff} = 0.25\ \mu m$, $W = 4x50\ \mu m$)

($V_{DS} = 3$ V, $V_G = 2$ V, $I_{DS} = 41$ mA)

Figure 32. Measured and modeled MAG/MSG behavior for the best performing MICROX FET which was characterized. The device structure included 4 x 50 micron wide gates with an effective gate length of 250 nm. The equivalent circuit component values for the model are also listed.



$F_t = 9.2$ GHz, $F_{max} = 20$ GHz

($L_{eff} = 0.40$ μm, W = 4x50 μm)

($V_{DS} = -4.0$ V, $V_G = -4.0$ V, $I_{DS} = 19$ mA)

Figure 33. RF performance of a 4 x 50-micron wide gate P-channel MOSFET with an effective gate length of 400 nm indicates the feasibility of CMOS RF circuits.

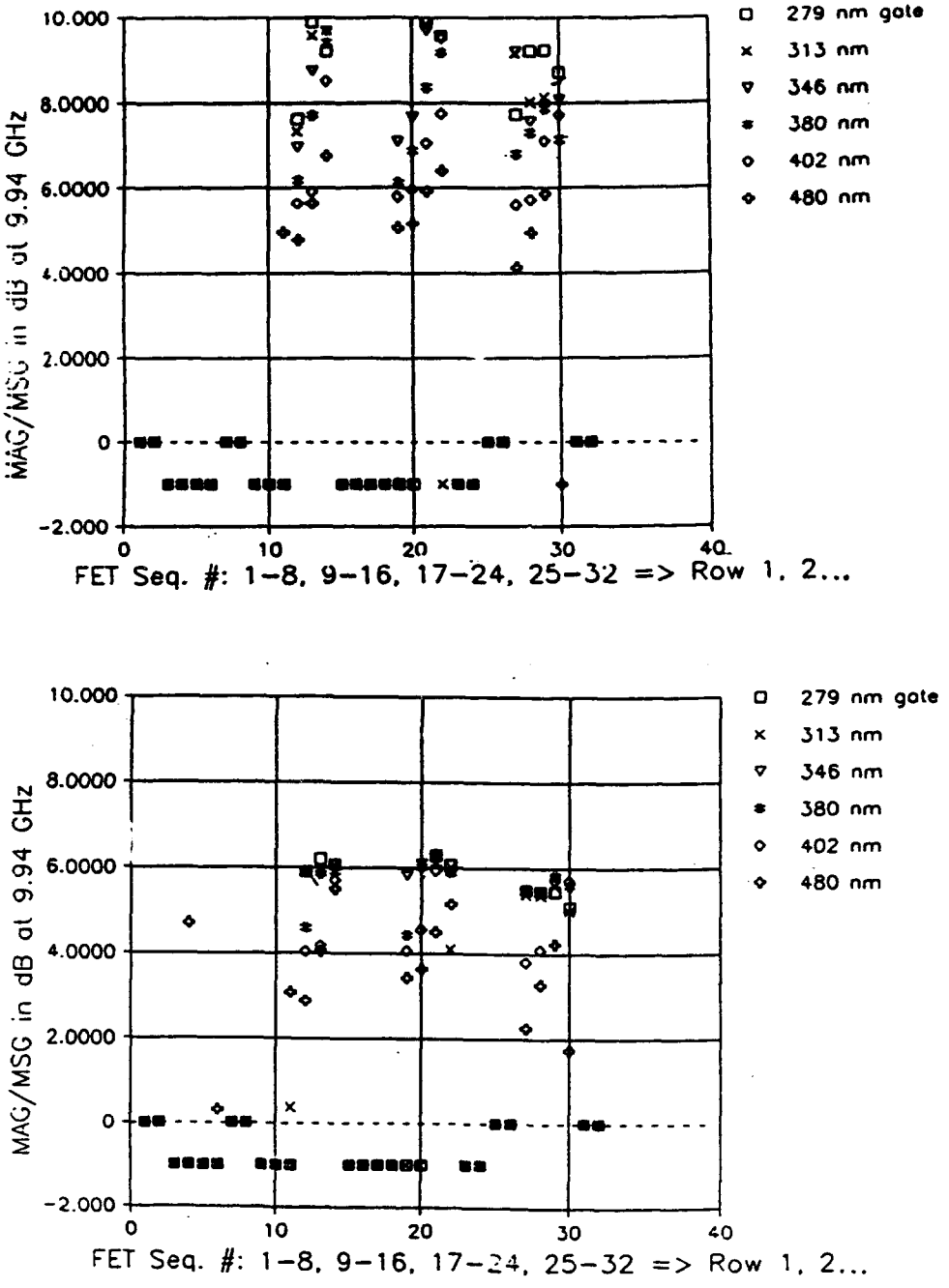


Figure 34. Improved gain performance of 4 x 100 μm-wide gate NMOSFETs after airbridging (top panel) compared to on-wafer probe results prior to airbridging (bottom panel. There was about 3.8 dB improvement in devices with the shortest gates.

channel which were not previously accessible. Generally this increased the gain of the longest channel (480 nm) FETs by about 1.8 dB. For devices with shorter channel lengths, the average improvement in gain was progressively more. Improvements over the pre-airbridge gain values at 9.95 MHz were 2.3, 2.5, 2.8, 3.4, and 3.6 dB for devices with final channel lengths of 402, 380, 343, 303, and 279 nm, respectively.

In addition to this general improvement in gain, the effect of airbridging was to provide some differentiation in the best gain for devices with gate lengths ranging from 279 to 380 nm, which was not present before airbridging. In this range of gate lengths, a 100 nm reduction in gate length is worth about 0.42 dB of gain for the best performing FETs. For longer gates (380 to 480 nm), the benefit is even greater. A 100 nm reduction in gate length yields about 2.7 dB in higher gain.

Devices with moderately long channels (>350 nm) from a wafer with a thicker channel (123 nm vs. 100 nm) and a heavier channel implant (2×10^{12} vs 1×10^{12} phosphorus ions/cm^2) than for the wafer previously discussed, exhibited improved RF performance features. There was less of a gradient in RF performance across the wafer, and the average gain was nearly 1 dB higher. These observations indicate that MICROX does not require structures with extremely aggressive geometries in order to provide performance adequate for many RF applications.

In RF applications of FETs, the power gain and efficiency are of concern. Power measurements were made on devices with various geometries of both the LDD and non-LDD types. The best result, shown in Figure 35, was 250 mW per mm of gate periphery for 8.45 dB of associated gain and 49% Power Added Efficiency (PAE) at 2 GHz. A non-LDD device with drawn gate length of 0.55 μm and a 4 x 100-μm gate structure provided this performance.

At 10 GHz the best power performance (Figure 36) was obtained from an LDD FET with an effective gate length of 1/4 μm. It delivered 60 mW/mm of gate periphery. The PAE was 19% and the associated gain, 4.6 dB for this device. These are the first results of silicon FET performance at such high frequencies.

4.1.3 Noise Characteristics

MICROX devices produced for this program have the lowest broadband noise yet reported for silicon FETs. Both LDD and non-LDD devices have been evaluated. The LDD structure increases the drain voltage capability and provides higher output resistance for short channel devices due to the interposition of the higher resistance LDD region between the drain contact and the active channel. Of necessity, increased resistance compromises noise performance, but the devices

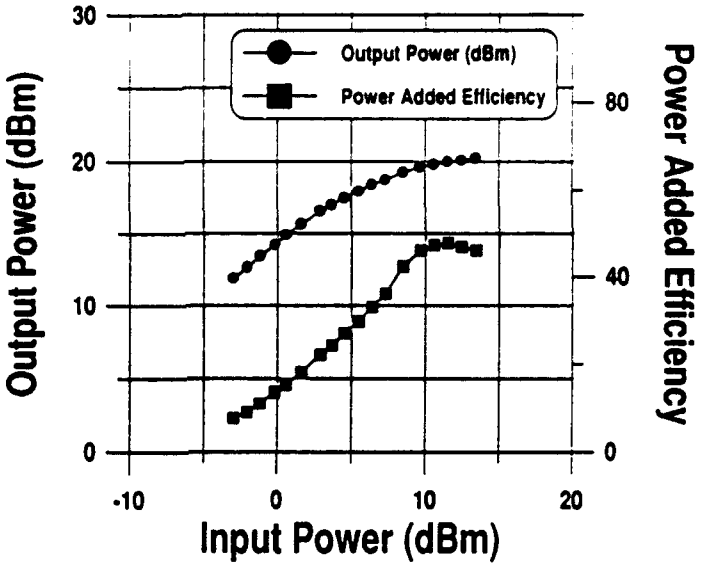


Figure 35. N-channel MICROX FET with 0.6 mm-long gate delivers 250 mW/mm output power at 2 GHz with nearly 50% Power Added Efficiency (PAE) and an associated gain of 8.5 dB.

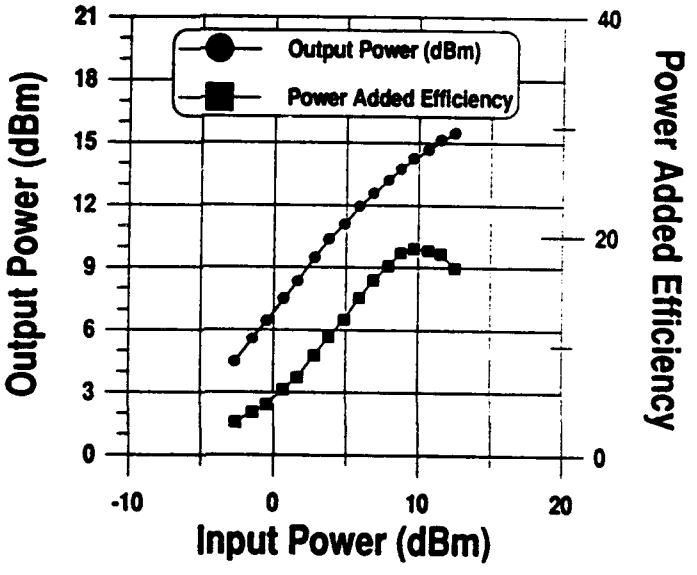


Figure 36. A MICROX FET with a quarter-micron gate and LDD operates at 10 GHz, providing 50 mW/mm of power at 19% PAE with 4.6 dB of associated gain.

fabricated for the program had a wide range of geometries which allowed assessment of the channel and gate finger design influences on noise behavior. For the LDD devices, a high fabrication yield permitted evaluations on a variety of geometric structures for a more complete view of an empirical route to optimizing noise performance. Non-LDD devices, with lower series resistance, gave the best noise performance, all other factors being equal.

Noise measurements were made using a type NP5B test set from ATN Microwaves, Inc. of Woburn, Mass. That equipment was used with an HP 8970B Noise Figure Meter, a HP 8515A S-parameter Test Set and an automatic wafer probe station. The generalized method has been treated by Gupta et al.[19] Equipment-specific issues of the measurement technique used for the current evaluation are described in the instructions for the NP5B test set.

The FET with the best broad-band noise performance had a non-LDD structure. This device had a noise figure of 0.8 dB, with 17.7 dB of assocated gain at 2 GHz, as shown in the top panel of Figure 37. The drawn gate length was 480 nm, and a 6 x 30-μm gate structure was used. Another device with the same gate length but a larger periphery (4 x 100-μm gate fingers) had a noise figure of 1.5 dB and 14.1 dB of associated gain at 2 GHz. The device results are used below to relate geometric influences on minimum noise.

For the LDD devices, the minimum noise figure was 1.33 dB with associated gain of 17.7 dB, as determined from measurement. The fitted value of minimum noise figure (lower panel in Figure 37) was just over 1.5 dB. The best result obtained on a Westinghouse MICROX FET before this program began was about 3 dB at 2 GHz.

For comparison purposes, consider noise results reported in the recent literature for other high frequency silicon MOSFETs. BESOI (Bonded and etched Back Silicon on Insulator) FETs gave minimum noise figures of 5.0 dB at 2 GHz, with an associated gain value of 6.4 dB, as reported by Caviglia et al.[10] For bulk N-MOS devices in a 50 ohm-cm substrate, Raynaud et al.[11] reported a minimum noise figure of 5.3 dB at 8 GHz (about 2.2 dB higher than for MICROX) with an associated gain value of 4.6 dB (3.4 dB lower than for current MICROX).

Extensive measurements of broadband noise characteristics were made on LDD devices, whose specific geometric differences allow assessment of gate geometry influences on noise behavior. The results are given in Table 4. Figures 38 and 39 show the influences on noise performance of channel length, gate finger width, and number of gate fingers.

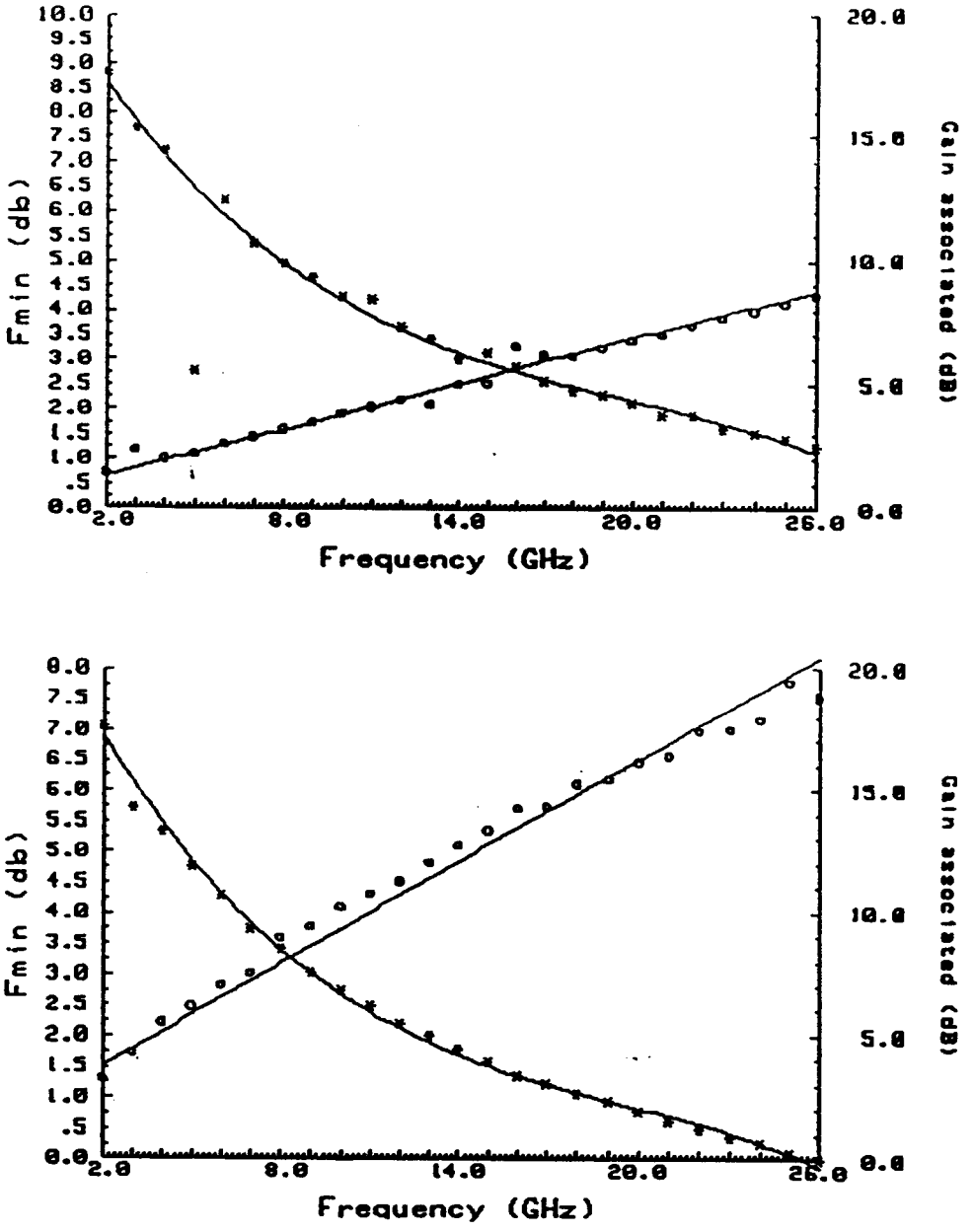


Figure 37. Broad band noise performance of MICROX FETs is enhanced in structures without a Low Doped Drain (top panel) compared to those with an LDD (bottom). Shown are measured (points) and fitted (lines) behavior of minimum noise figure and associated gain from 2 to 26 GHz.

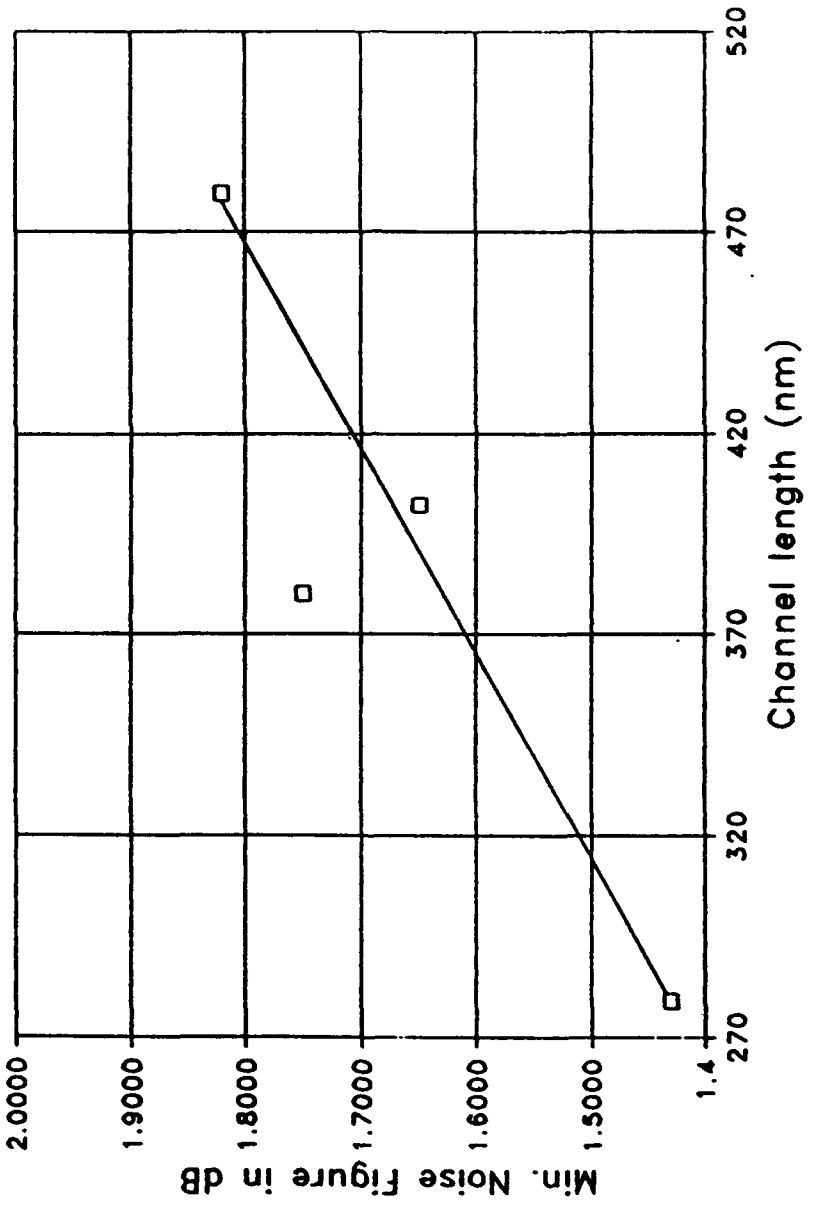


Figure 38. The minimum noise figure at 2 GHz follows a linear dependence on drawn gate length for non-LDD MICROX FETs with a 4-fingered, 50 micron-wide gate geometry.

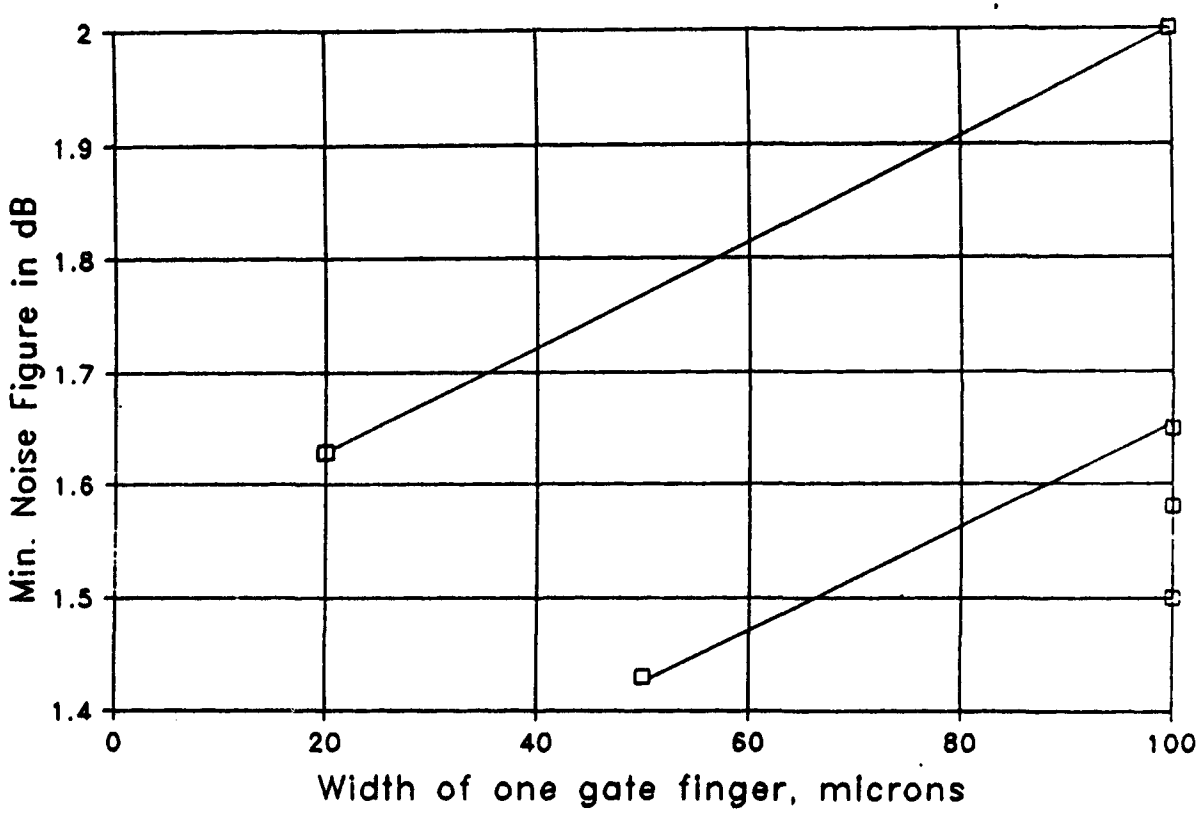


Figure 39. Minimum noise figure at 2 GHz increases with individual finger width for both 4- (lower) and 6-fingered (upper) gate structures in non-LDD MICROX FETs.

The influence of gate length on noise figure for these devices is straightforward, as shown in Figure 38. Devices with shorter channel lengths have higher gain, which is reflected in lower noise. For the devices in question, which were designed with low doped drain structures for higher drain voltage capability, the sensitivity of noise figure (at 2 GHZ) to channel length is 0.2 db per 0.1 μm of drawn gate length.

Figure 39 illustrates the direct effect of increased gate resistance along gate fingers as their width is increased for the cases of 4- and of 6-fingered gate designs. The indicated sensitivity of noise figure is 0.45 dB per 100 μm of gate finger width (of a single finger). As more fingers are added in parallel (e. g. of 100 μm-wide fingers), the noise figure increases, probably because the device gain suffers from non-commensurate increases in parasitic gate capacitance with respect to transconductance. In the case of the 100-μm-wide gate fingers, the penalty is about 0.18 dB per added gate finger in going from 4 to 6 fingers.

The influence of the number of gate fingers in terms of the relative scaling of parasitic gate capacitance and transconductance is not straightforward, as seen from the Group III information in Table 3. Here, FETs with 20 μm-wide gate fingers show improved noise performance as the number of gate fingers is increased from 2 to 6, presumably because the capacitance overhead of the gate pads is used more effectively for higher gain as the number of fingers is increased. For the 100 μm-wide fingers, (as noted in connection with Figure 39) there is a benefit from better use of the gate pad capacitance with 4 fingers (400 μm of total active periphery).

The noise results do not show a simple dependence on the number of gate fingers, instead the total gate width, appears to be significant. Figure 40 suggests that optimum noise performance for the LDD devices with 279 nm gate lengths would be delivered with a total gate width of 200 to 300 μm.

The following list of points summarizes the main geometric effects on noise performance of MICROX FETs studied on this program:

1. With fixed gate finger geometries, devices having shorter channel lengths produce higher gain, and hence lower noise.

2. With short, fixed (279 nm drawn) gate length, the noise figure increases due to increased gate resistance along the gate fingers as their width is increased for both 4- and 6-fingered gate designs.

Table 4. SUMMARY OF MINIMUM NOISE FIGURE RESULTS AT 2 GHz FOR NON-LDD DEVICES WITH VARIOUS GATE GEOMETRIES

Location Designation X	Y	Gate length	Gate Config.	Minimum noise fig. (dB) meas.	fitted	Associated Gain (dB) meas.	fitted
Group I - Gate length variation							
5	3	480 nm	4 x 50 μm	1.73	1.82	16.62	16.66
5	3	402 nm	4 x 50 μm	1.71	1.65	16.42	15.00
5	3	380 nm	4 x 50 μm	1.76	1.75	16.82	15.80
5	3	279 nm	4 x 50 μm	2.17	1.77	19.41	13.80
Group II - Gate finger width influence, 4- and 6-finger arrangements							
5	3	279 nm	6 x 100 μm	2.21	2.00	16.05	15.20
5	5	279 nm	4 x 100 μm	1.33	1.58	17.65	17.00
5	5*	279 nm	4 x 100 μm	1.24	1.50	18.04	17.20
5	3	279 nm	4 x 100 μm	1.68	1.65	17.4	17.00
5	3	279 nm	4 x 50 μm	1.52	1.43	17.66	16.10
5	3	279 nm	6 x 20 μm	1.85	1.63	16.50	15.60
Group III - Finger number influence for 20- and 100-μm finger widths							
5	3	279 nm	6 x 100 μm	2.21	2.00	16.05	15.20
5	3	279 nm	6 x 20 μm	1.85	1.63	16.50	15.60
5	3	279 nm	4 x 100 μm	1.68	1.65	17.4	17.00
5	3	279 nm	4 x 50 μm	1.52	1.43	17.66	16.10
5	3	279 nm	2 x 20 μm	2.17	1.77	19.41	13.80

*Repeat measurement on previous device

3. At fixed finger width, as more fingers are added in parallel (e. g. of 100 μm-wide fingers), the noise figure increases since gain suffers from increases in parasitic gate capacitance.

4. For a given gate length, minimum noise can be obtained if a wide range of gate periphery is considered to allow minimization of parasitic capacitance with respect to transconductance as gate periphery is varied. For the LDD devices with 279 nm gate lengths, the minimum noise figure would be expected with a total gate width of 200 to 300 μm.

The broadband noise performance of FETs generally benefits from features intended to increase the frequency capability of devices. Table 5 summarizes the noise performance at 10 GHz of the various devices with the highest frequency capabilities which were produced and characterized on this program.

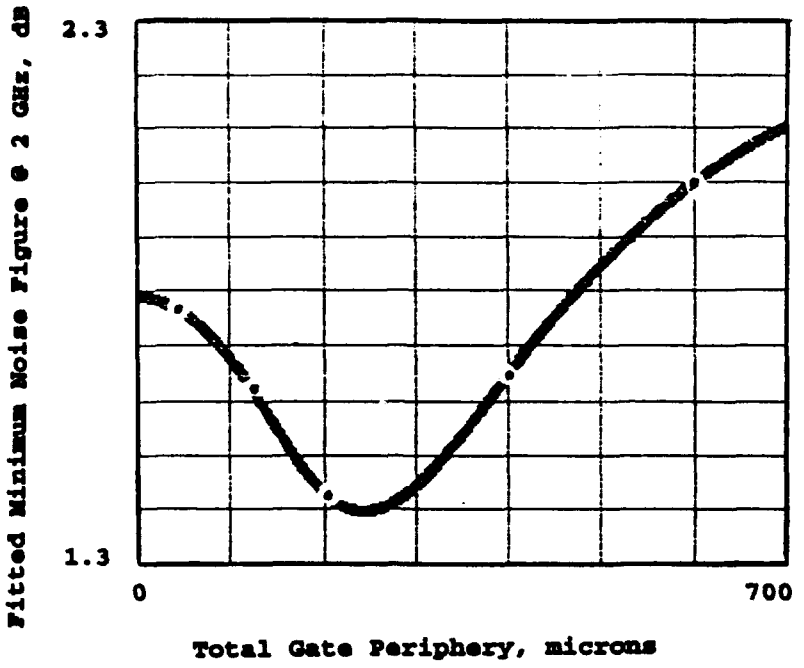


Figure 40. A minimum value for the noise figure is indicated when a wide range of gate periphery values is considered for 279 nm gate FETs without LDDs, resulting from an optimum tradeoff between transconductance and parasitic capacitance.

Table 5. SUMMARY OF BEST SMALL SIGNAL FREQUENCY PERFORMANCE AND NOISE RESULTS FROM MICROX DEVICES.

Type	LDD	f_{max} *	f_t **	NF_{min} @ 10 GHz
n-channel	No	42 GHz	24 GHz	2.0 dB
p-channel	No	20 GHz	9 GHz	3.6 dB
n-channel	Yes	32 GHz	25 GHz	3.4 dB

* Maximum oscillation frequency, giving unity power gain.
** Cut-off frequency, giving unity short circuit current gain.

4.2 Processing Technology

The three topics of this section highlight process issues which are important to the realization of practical RF circuits with MICROX. The first, circuit planarization, is critical to guarantee interconnect continuity. This is especially true in the case of the multiple gate fingers as they are brought off the device mesa to the common gate buss.

Formation of metal-insulator-metal capacitors is another important capability which is required for MICROX MMICs. A key feature of the capacitor processing approach has been to use a rejection process to remove the capacitor dielectric from all areas except the capacitor plates. This facilitates the interconnection of devices without the need to etch local contact holes through the dielectric layer to reach the first level metallization layer.

Processing for through-the-wafer vias on MICROX wafers thinned to 100 microns is critical to the MICROX demonstration circuits, since the designs require microstrip interconnect lines. As in the case of RF FET designs, the background in GaAs via processing was used to provide the basic fabrication approach, with modifications made to accommodate the material and structural differences of the two technologies.

4.2.1 Planarization

Planarization requires special attention in the case of silicon-on-insulator (SOI) structures such as MICROX, since isolation of individual devices is relatively easy by removing the top silicon layer except in the areas of so-called active device mesas. It requires considerable attention, however, to provide a process sequence which will minimize potential discontinuities in the top surface of the wafer which could break interconnect metal. This is of particular concern in regions crossed by the gate reinforcement metal.

The planarization process which was applied to the wafers containing MMICs involves a sequence of additive and subtractive processes. Effects of the processing are shown schematically in Figure 41. The process step numbers for each view refer to the processing described in Table A.2 of Appendix A. Figure 42 shows a comparison of typical surface profiles, before and after the planarization sequence, for the worst case among the six wafers which were processed. There was a step of about 213 Angstroms from the field area down to the silicon device mesa. Measured steps on the other wafers ranged from zero to 150 Angstroms.

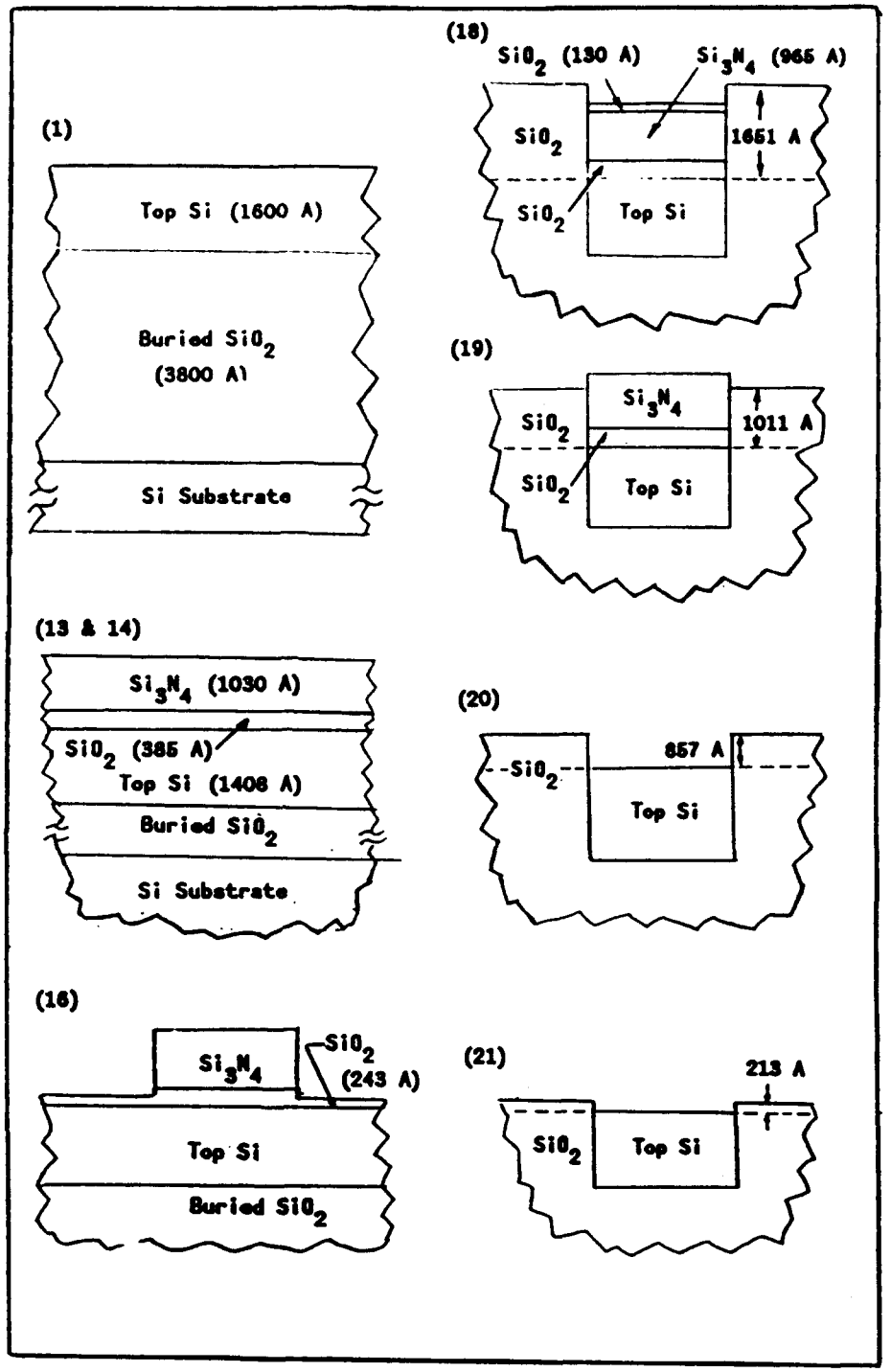
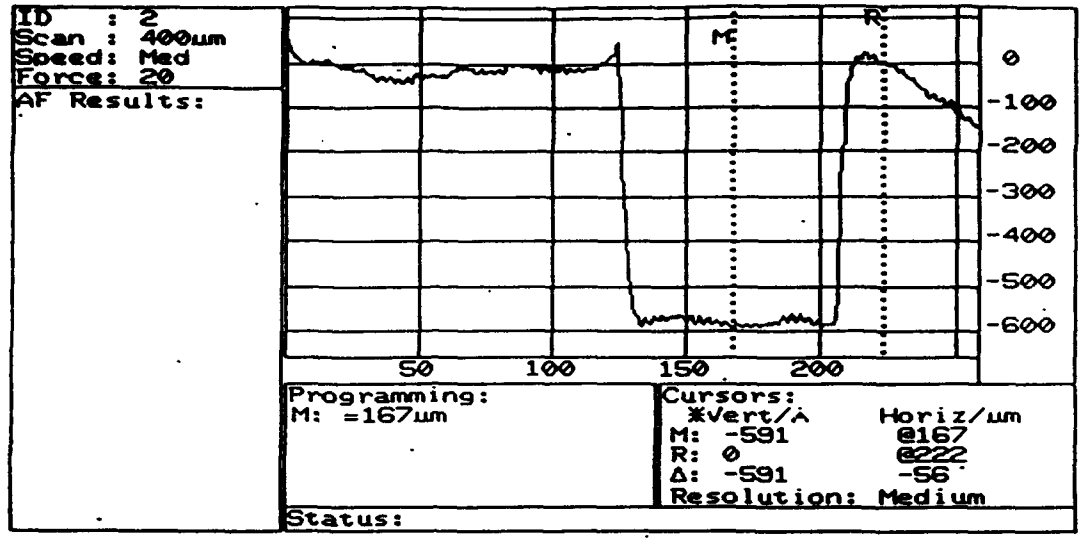


Figure 41. A schematic view of the results of key steps in the planarization process (for a final nominal step height of 213 A) to provide islands of silicon for fabricating individual FETs to be combined in a MICROX IC or MMIC. The numbers in parenthesis for each view refer to the step in the processing sequence given in Table A.2 of Appendix A.



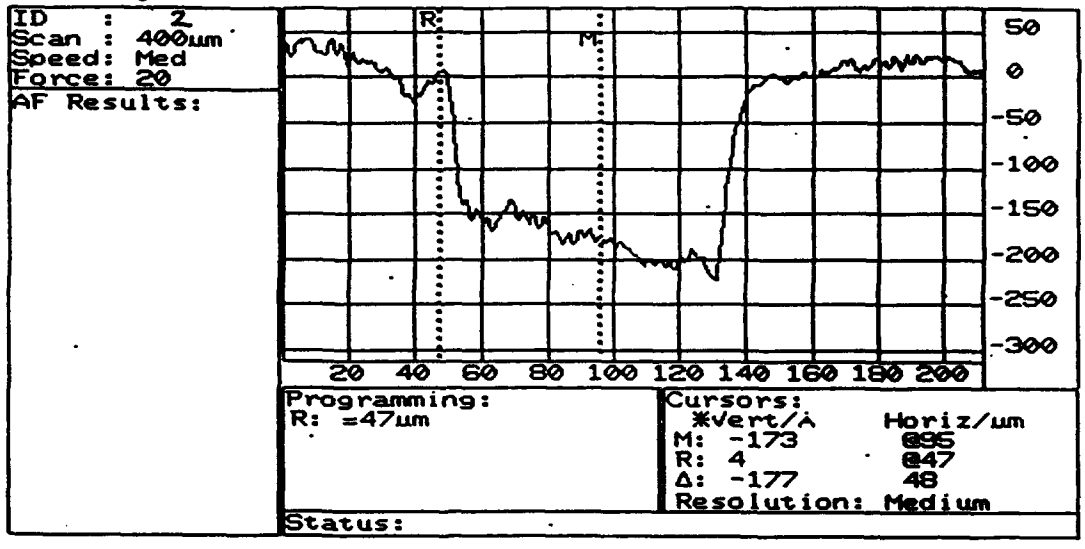


Figure 42. Example of the largest silicon-to-field oxide step measured after the wet etch step in planarization (bottom panel) of the MICROX in the final fabrication lot. For comparison, the top panel shows the profile after the preceding step of silicon nitride removal by reactive ion etching.

4.2.2 Capacitors

The capacitor process details for MICROX were chosen after reviewing in-house GaAs MMIC processing for capacitors. At Baltimore, a major concern is that the silicon nitride dielectric adequately passivate the gate/drain region of GaAs MESFETs. To satisfy this requirement, an electron cyclotron resonance deposition process at a temperature above 100 C is used. At Pittsburgh, two processes have given comparable capacitor results for GaAs applications. Silicon nitride films from both remote plasma (higher temperature) and plasma-enhanced (below 100 C) chemical vapor deposition (PECVD) processes have provided adequate specific capacitance and low loss. The latter process was chosen for MICROX since its lower temperature would facilitate liftoff in lithographic processing to define the dielectric area.

The capacitor plate metallization details for MICROX and for GaAs differ slightly, but similar gold and chromium layers are used beneath the nitride. At Baltimore the bottom capacitor plate metal is Ti (1000 A)/Au (4000 A)/ Cr (200 A). The earlier use of Pt under the Au layer has been dropped because "spitting" during its evaporation has been implicated in "seeding" the growth of spikes in the subsequently deposited gold layer. At Pittsburgh, GaAs MMIC capacitors use a bottom metal plate consisting of Ti (1000 A)/Pt (400 A)/Au (4100 A)/Cr (200 A). In both of these cases, the nitride deposition is made on a 200 A-thick Cr adhesion-promoting layer which overlays the Au layer (about 4100 A thick) for low in-plane resistance.

For MICROX the approach has been to apply the lower capacitor plate metal using evaporation methods: 500 A of Cr (for adhesion to the field oxide), followed, *in situ*, by either 500 or 1000 A of Pd as a diffusion barrier. Subsequently, 3500 A of Au is deposited by electron beam evaporation. Heating of the resist pattern, which can occur with sputtering of the Cr and Pd layers, is avoided. Easy rejection of the resist and metal defines the interconnect metal, the contacts to the active devices, and the capacitor bottom plate.

Before deposition of the silicon nitride dielectric, a 200 A-thick layer of Cr was evaporated to aid adhesion in the capacitor areas. A pattern for nitride rejection was applied, followed by PECVD of the capacitor dielectric, then the resist pattern with the excess nitride were rejected. This produced good nitride adhesion on both the oxide and the chromium-over-oxide bands surrounding the Metal-1 portion of the lower capacitor plates. The nitride did not adhere in the main dielectric areas having Cr over Metal-1, regardless of the size of the capacitor.

Two possible causes were identified for the lack of nitride adhesion. Either the thin (<300 A) Cr layer reacted with the underlying

gold surface of the Metal-1 contact or residues from the photoresist processing immediately before the nitride deposition step interferred with adhesion of the nitride.

An experiment was designed to elucidate effects involving Pd and resist processing under four conditions:

Case I	Common rejection of a thick (1000 A) Pd barrier layer under Cr with separate rejection of nitride,
Case II	Common rejection of (thick) Pd/Cr/nitride,
Case III	Common rejection of Cr and nitride without Pd, and
Case IV	Common rejection of thin (300 A) Pd, Cr, and nitride.

Cases III and IV produced successful results. The key was common rejection of the adhesion-promoting film and the dielectric layer. Reliable adhesion of the nitride was achieved if there was no photoresist processing immediately before the nitride deposition.

The use of a thick Pd layer under the chrome produced problems by causing the lifting of the masking resist layer. In Case I this occurred spontaneously but only immediately after the metals were deposited, since there was no indication of spuriously metallized areas. In Case II, there was no resist lifting until the nitride deposition process was underway. This indicates that rejection of a thick Pd layer, alone or in conjunction with a dielectric overlayer, is not acceptable for MICROX capacitor processing.

Case I, involved separate delineation of the capacitor dielectric. The capacitor dielectric areas over the Metal-1 areas were not adherent during the final photoresist rejection step. This was similar to the initial observations. Case III produced adherent nitride in capacitor dielectric areas, following common rejection of the Cr adhesion film and the nitride. All capacitor areas were well delineated, regardless of size or shape. Similar results were obtained with Case IV, using a thin Pd layer beneath the Cr film, but to simplify processing this approach was not used in the MMIC wafers.

4.2.3 Via Processing

Processing of vias on MICROX wafers thinned to 100 microns is needed for the MICROX demonstration circuits, to implement microstrip interconnect lines. Although expertise in the via area was developed at

Table 6. STEPS REQUIRED TO COMPLETE MICROX MMIC WAFERS AFTER FRONT SIDE CIRCUIT PROCESSING

1	Apply protective resist to top surface
2	Mount wafer to carrier for thinning
3	Lap from back to 100 microns thickness
4	Polish lapped surface
5	IR aligner: Mask 15, window for via mask alignment
6	Evaporate 5000 A Al, for RIE protection layer
7	Lift off Al in mask window areas
8	IR aligner: Mask-12C, via pattern
9	Wet etch via pattern in aluminum
10	Remove resist from aluminum
11	RIE vias (with SF_6) to buried oxide
12	Inspect vias
13	Wet etch to remove all aluminum
14	RIE oxide inside vias using $CHF_3 + O_2$
15	Inspect vias
16	Etch Cr oxide/Pd with $BCl_3 + Cl_2$ to expose Au
17	Inspect vias
18	Sputter Ti/Au as plating base
19	Electroplate vias, backplane
20	Demount wafer from carrier
21	Strip wax, resist from front surface

Westinghouse for GaAs MMICs, specific MICROX issues required resolution. Table 6 lists the processing steps for thinning, via processing, and plating, which should aid in understanding these issues.

First, the circuit side of the wafer, with its airbridges, must be protected (Step 1). After mounting to a support wafer covered with a high melting-temperature wax and thinning (Step 3), the circuit wafer surface must be polished. This allows for alignment, exposure, and development (Step 5) of a pre-alignment mask on the back surface to define areas to be protected from the subsequent aluminum mask layer deposition (Step 6). (These selected areas are kept open to permit later aligning of the via mask with via metallization patterns on the top surface.) The aluminum areas to remain are defined by standard

Figure 43. SEM view of silicon vias after Reactive Ion Etching (RIE) with preliminary operating parameters which caused pitting in Al mask and undercutting at via periphery. Etch depth, 95 mm.

resist lift-off in Step 7. Next, the via mask exposed is after it is registered to the circuit-side alignment marks which are visible in the previously defined areas. The via pattern is wet etched into the aluminum layer (Step 9), and the resist is stripped (Step 10). The aluminum pattern protects the back surface during reactive ion etching with sulfur hexafluoride (Step 11) of the vias. This etch is through the entire 4-mil thickness of the wafer to the buried oxide. After inspection, the aluminum mask is removed (Step 13).

The initial RIE etching conditions for the silicon produced unacceptable degradation of the aluminum mask. The aluminum eroded away much earlier than expected, resulting in a loss of pattern resolution. Additionally, this allowed silicon areas to be etched because of excessive pitting in the aluminum. Figure 43 shows a view of vias etched under the initial conditions. In addition to the aluminum pits, there was about 40 microns of undercutting or "lifting" of the aluminum mask around the edge of the via pattern. Adjustment of the RIE operating parameters, based on silicon wafer etching experience at Westinghouse-Baltimore, reduced the aluminum degradation (Figure 44a).

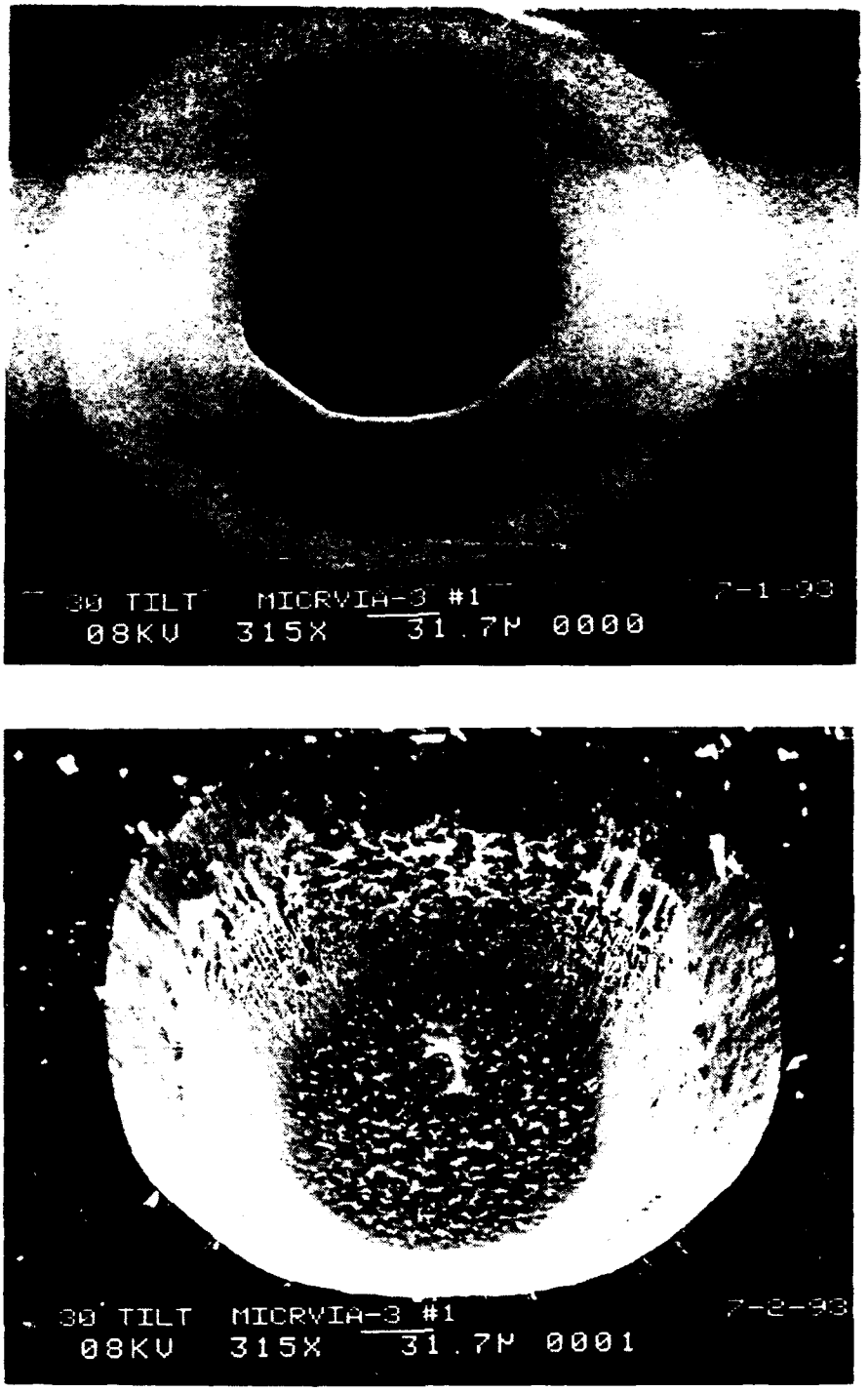


Figure 44. SEM views of silicon vias formed after modification of RIE conditions. (Top) Acceptable undercutting of the Al mask after etching 100 mm deep. (Bottom) After emoval of Al masking layer.

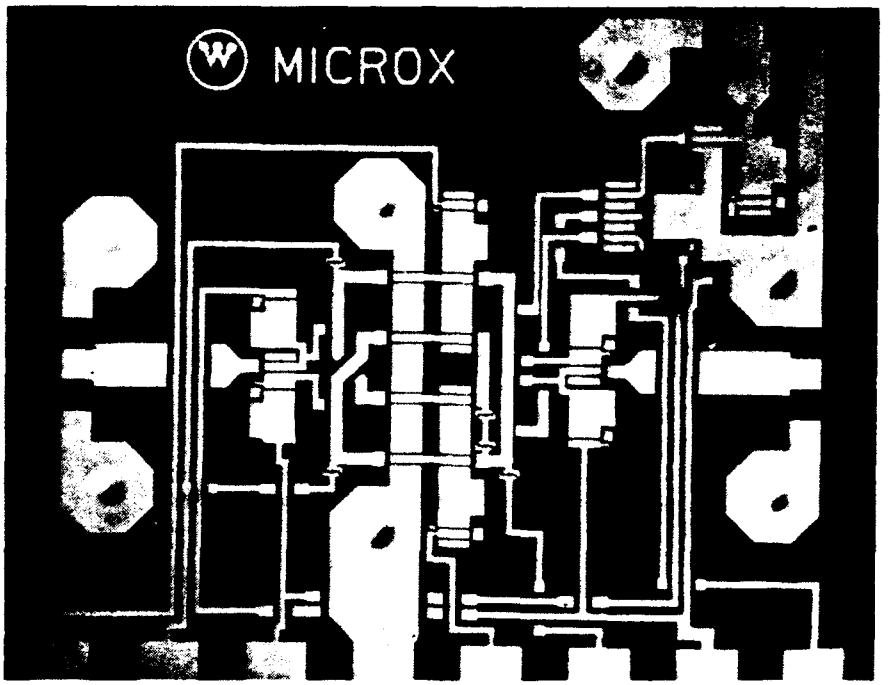


Figure 45. Microphoto showing deformation of thin (3300 A) frontside circuit metal after RIE etching to form vias from the back of the wafer. The deformation illustrates the alignment of the backside vias to the front side ground pads.

There was less undercutting of the mask and a smoother silicon surface resulted, as shown in Figure 44b after removal of the Al mask layer.

To complete the vias after etching through the silicon wafer, the silicon dioxide layer that remains under the circuit-side metal pads must be removed by reactive ion etching with $CHF_3 + O_2$ (Step 14). Final etching through the Cr and Pd layers underlying the gold of Metal-1 is done using $BCl_3 + Cl_2$ (Step 16). A Ti/Au layer is uniformly deposited over the backside to form the ground plane. It must also cover the walls of the vias and the exposed gold of Metal-1 over the vias. The final step is the Au plating process to provide a thickness adequate for subsequent chip mounting.

Several via test samples were processed initially to verify the processing steps. The front, or circuit side, of these test samples was prepared only with the 3300 angstrom-thick first metal pattern, to generate samples quickly. Although the samples were satisfactory for establishing the process steps, the first metal pattern was deformed after the RIE via etch, as shown in Figure 45. In this case, the deformation clearly shows the excellent alignment between the front side and back side patterns. Deformation would not be a problem with the plated circuit-side metal which is at least 5 microns thick.

This via processing effort was successful in establishing conditions permitting processing of several MICROX MMIC wafers. However, the processing is not adequately controlled to allow processing a large lot of wafers to a single set of specifications. As it stands, the process requires extensive monitoring of intermediate etching results for the silicon and the Metal-1 sublayers. This monitoring is needed because of the sensitivity of etch results to the geometry, undercutting, and layered materials associated with the deep vias.

4.3 Circuit Performance

The designs of the MICROX demonstration circuits are based on using microstrip interconnections. This requires that the circuit wafers be thinned to 100 microns and provided with a groundplane accessed through vias at selected locations in the circuits. On the wafers completed through this stage of processing, higher than expected resistance was encountered in the source/drain contacts and along the gate fingers. The digital attenuator design is sufficiently robust to overcome these problems and preliminary measurements demonstrate operation of the attenuator switch components. On the basis of this, MICROX MMICs incorporating digital control logic are feasible L- and S-band systems. For the remaining circuits, problems in achieving low resistance gate contacts on the thinned wafers with microstrip, precluded making measurements.

4.3.1 Digital Attenuator Characteristics

Figure 46 shows attenuation and minimum loss behavior for 1, 2, 4, and 8 dB attenuator test bits which were included as a part of the mask design for the MICROX MMICs on this program. The measured attenuation deviates from the design because of higher source and drain contact resistance than expected for the design. The attenuation behavior exhibited in Figure 46 could be accommodated and used in the four-bit attenuator design. These preliminary results show that MICROX attenuators with this design should be operable out to at least 10 GHz.

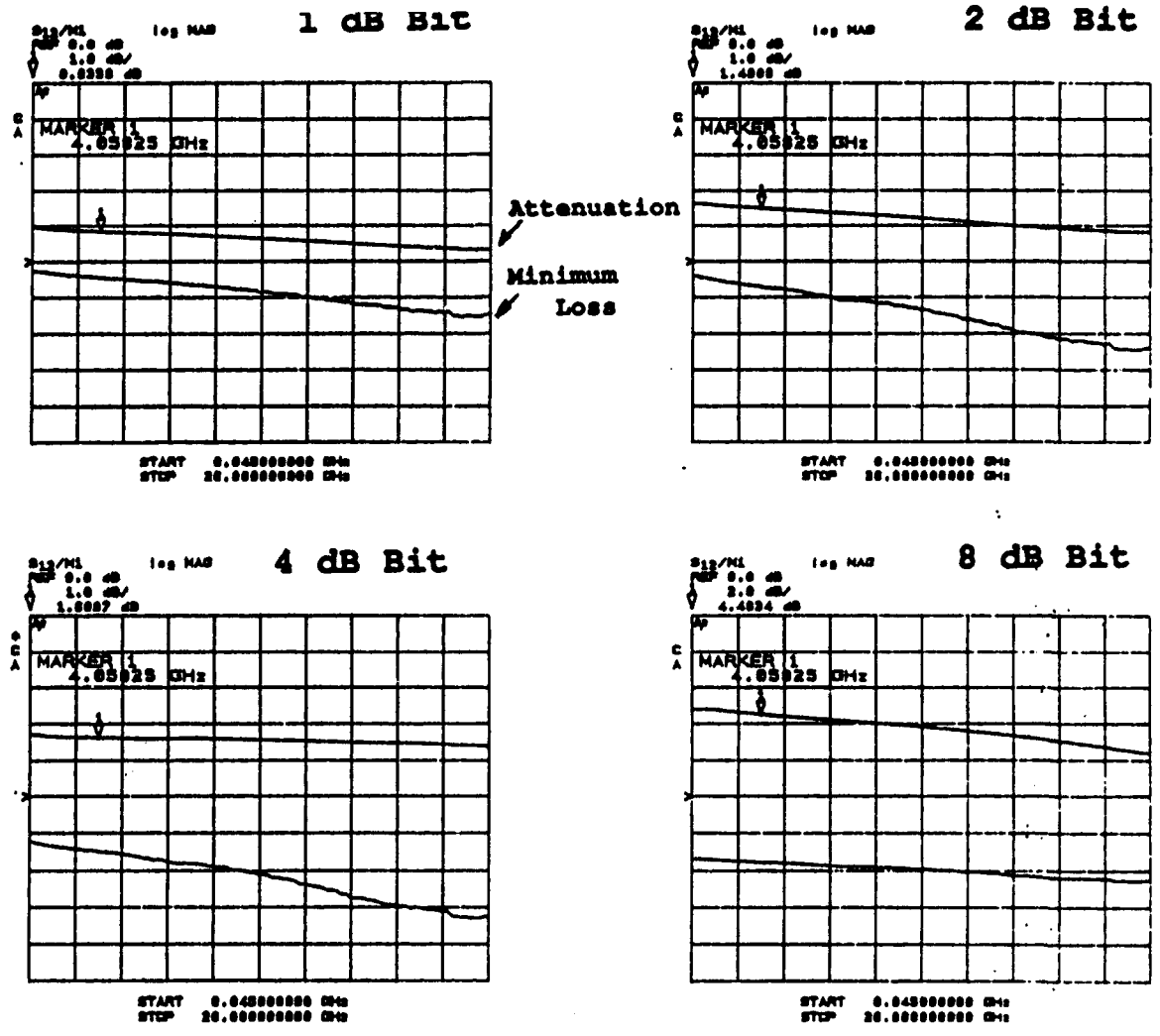


Figure 46. Examples of the measured attenuation (upper curve in each case) and minimum loss (lower curve) characteristics of MICROX digital attenuator bits.

5. DISCUSSION

The MICROX processing, device, and circuit design efforts on this program demonstrate good prospects for realizing RF MMICs with silicon IC technology. Current MICROX device capabilities are adequate for circuit demonstrations and co-integration of RF and digital functions. Some additional process development, especially as regards contact producibility, is needed. Selected foundry demonstrations involving RF circuits can be considered and a realistic economic assessment of large scale MICROX circuit manufacturing made.

5.1 Major Accomplishments

5.1.1 Processing results

As a part of the fabrication approach, electron beam delineation of the gate has been used throughout the program. This has provided two major benefits for this effort. First, definition of quarter-micron gates has become a routine matter, even for the production of large periphery structures. Additionally, deliberate on-wafer variation of gate length has been possible to explore the sensitivity of RF device performance, including noise behavior, to geometry. With this E-beam experience in hand, it is now possible to select a specific gate length and use photolithography for subsequent fabrication effort.

A major issue with silicon-on-insulator device structures in the limit of very short gate lengths is the sensitivity of device behavior to variations in channel thickness. Such variations are unavoidable by the nature of the oxygen implantation process used to prepare the MICROX material for this program. In the case of microwave devices, the ultimate criterion of their utility is performance. This is influenced by many structural and design aspects that depend on the material uniformity. Because of the complexity of this issue, on this program the approach has been to characterize RF performance as a function of position. Maps of performance variations over a wafer aid in estimating the impact of uniformity on yield of devices from a given wafer.

At the start of this program there was strong emphasis on realizing MOSFET gate lengths in the quarter-micron range for high frequency performance. That work was successful. It indicates that MICROX devices are feasible for applications extending into X-band. Even at lower frequencies, short gates provide significant benefits in terms of improved noise performance. It subsequently became clear that MICROX FETs with gates in the half micron range were also very useful and more readily realizable with near term manufacturing capabilities to satisfy many applications in L- and S-band.

After gate delineation, one of the most critical issues in microwave FET fabrication is achieving minimum resistance for the source/drain and the gate regions of the device. This involves contact as well as conductor line resistance. Addressing these issues is more difficult than simply adapting technology from the silicon digital device area. There aluminum metallization, which can be alloyed into silicon in the presence of thin silicon oxide layers remaining after etching, has been adequate. RF devices require accommodating relatively thick gold, as well as multiple layers which may include Cr, Ti, and Pd, in the contact scheme. To compound the difficulty, these metallization alternatives require oxide-free silicon contact surfaces for low resistance. It is clear that extension of silicon FET RF performance in devices fabricated with more involved contact and conductor processing steps will require better process diagnostic and evaluation capabilities than are presently considered routine.

Two key processing capabilities, needed to implement MICROX RF FETs and circuits, have been developed and demonstrated on this program: accommodating airbridge interconnections for large periphery devices and providing Metal-Insulator-Metal capacitors with silicon nitride dielectric for RF use. The latter has been accomplished with lift-off methods which retain the nitride in selected areas only. In this way the process can be applied to circuits using single level interconnect metallization, which is compatible with the local crossovers afforded by electroplated airbridges.

5.1.2 Device Advances

Effort on this program has produced a number of major device-related accomplishments, as silicon frequency capability has benefitted from the reduced junction and device parasitics afforded by MICROX. These accomplishments include:

- Demonstration of complementary RF FET fabrication in MICROX;
- Characterization of a variety of FET performance capabilities, important in applications, as a function of gate length and periphery;
- Best broadband noise results reported for silicon MOSFETs;
- Demonstration of multi-gate MOSFETs with 250 mW/mm power per unit periphery for L/S-band uses;

- Extraction of GaAs-FET-like small signal equivalent circuit models for MICROX devices;

- Determination of perimeter scaling factors for equivalent circuits to implement RF circuit designs.

During the program, a question arose concerning the operating temperature cability of MICROX devices with agressive geometries because of the buried silicon oxide layer. Its thermal conductivity is about a factor of ten lower than that of silicon. This issue is treated in Appendix C, which explores the thermal consequences of two different designs: the moderately long source and drain contact regions typical of GaAS microwave power FETs, and the dense packing typical of digital circuits. Typical power dis ipation of 10 W/cm of gate length would cause a manageable, maximum temperature rise of only 18 to 30 degrees in a MICROX RF device.

6. SUGGESTIONS FOR FUTURE WORK

Three areas of continuing effort can be identified now for particular benefit in the development of MICROX: near-term applications, yield, and new devices.

6.1 Applications

Generally, a competition between MICROX and GaAs MMICs or silicon bipolar circuits on broad grounds of performance and cost will be decided in favor of the incumbent technology. Data on performance, cost, reliability, etc. will be readily available for the established technology and most users will be reluctant to select a new technology on the promise of future benefits. In such a climate, the best opportunities for MICROX insertions are in near-term applications where cost reductions over GaAs parts are feasible using silicon manufacturing and integration capabilities. Projected yield will be an issue, of course, but it usually will be secondary to consideration of cost.

A consequence of this view is that niche applications for MICROX are the best initial targets. This can be an advantage, because the focus on the competing technology can be narrowed, with specific parts, cost, and performance identified. Once MICROX capability for the application is established and accepted, the argument for cost and yield benefits can be made, using an approach which follows the arguments made by Skinner[17] for using GaAs devices and MMICs. Progressive improvements in cost and yield can be handled as MICROX parts volume is projected to build during advanced development, pilot production, and full or foundry manufacturing.

Insertion opportunities for MICROX are suggested by a consideration of the current approaches to combine GaAs and Si capabilities in Multichip Modules (MCM) or exploit the capabilities of either separately, by expanding their respective historical roles.

6.2 Yield

Identifying and understanding issues of MICROX yield is very important, since the competing silicon bipolar and GaAs FET technologies are well characterized in this regard. Furthermore, these competitors have benefitted from production volume and experience to drive their yield-improvement efforts.

The yield of MICROX circuits cannot be treated as an isolated issue. In the absence of volume applications, adequate yield data will be slow in coming. Without an acceptable baseline for yield, potential users of MICROX will not readily commit to its use. Pilot production efforts on specialized MICROX parts would provide an ideal opportunity to realistically address MICROX yield. Such an effort should treat the

basic SOI formation process and the uniformity of the SOI structure. Adequate attention should be given to the yield impact of mesa, rather than junction, isolation with MICROX since it simplifies processing.

Enhanced speed/frequency performance is a major MICROX feature and future applications should draw the technology in that direction. Variability of SOI devices with aggressively short channel lengths should be treated as a yield matter in that context.

6.3 New Structures and Devices

As initially conceived, MICROX uses a subset of silicon technology capabilities, as a Silicon-on Insulator approach with a very high resistivity substrate, to offer MOSFET circuits similar to GaAs FETs in their capabilities below X-band. In this form MICROX offers easy combination of RF FET functions with digital control circuits and memory capabilities, drawn from the silicon digital area.

One of the acknowledged deficiencies of both MOSFETs and GaAs FETs in RF applications is limited output current driving capability. With conventional silicon, bipolar transistor and CMOS capability are combined in the BiCMOS approach as an integrated, supplemental solution to this problem at lower frequencies. This approach should apply for MICROX, also. It will require some accommodation in the bipolar designs for the reduction in minority carrier lifetime of the active silicon layer caused by the oxygen implant and annealing processes. Future MICROX development could profit from using BiCMOS for both RF and off-chip digital signal drive applications.

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APPENDIX A
MICROX CMOS AND NMOS PROCESSING SEQUENCES

The steps which were used to process complementary MICROX FETs on this program are described in Table A.1. Table A.2 gives the sequence of processing steps which were for used to fabricate MICROX demonstration circuits based on NMOSFETs.

Table A.1 -- SUMMARY OF MICROX CMOS FET PROCESSING SEQUENCE

	STEP	DESCRIPTION
00	RUN SUMMARY	Summarize and describe test pieces
01	MASK DESCRIPTION	Describe masks used in run
02	WAFER PREPARATION	Describe run wafers and splits
03	OXIDATION	Thin selected wafers to 1500 A Si
04	OXIDATION	Thin selected wafers to 1300 A Si
05	OXIDATION	Thin selected wafers to 1000 A Si
06	WET ETCH - OXIDE	Thin wafers by removing oxide
07	E-BEAM ZERO LEVEL	Define globals & DSW alignment marks
08	RIE - SILICON	Etch marks into silicon
09	STRIP RESIST	
10	OXIDATION	Oxide for stress relief and screen
11	DSW - NCH_LOAD_AS	For n-type implant into NCDM[1] transistors
12	ION IMPLANT PHOSPHORUS	Implant phos into NCDM transistors
13	STRIP RESIST	
14	DSW - PCH_THRESHOLD_As	For n-type implant into PCEM[2] transistors
15	ION IMPLANT PHOSPHORUS	Implant phosphorus into PCEM transistors
16	STRIP RESIST	
17	DSW - NCH_THRESHOLD_B	For boron implant into NCEM[3] transistors
18	ION IMPLANT BORON	Implant boron into NCEM transistors
19	STRIP RESIST	
20	ANNEAL - NITROGEN	Anneal channel implants
21	LPCVD - NITRIDE	Deposit nitride as an etch mask
22	DSW - MESA	Mask to define mesas
23	RIE - NITRIDE	Etch mesa patterns
24	WET ETCH - OXIDE	Etch screen oxide

Notes:
1. NCDM = n channel depletion mode
2. PCEM = p channel enhancement mode
3. NCEM = n channel enhancement mode.

Continued

Table A.1 -- (Continued)

	STEP	DESCRIPTION
25	STRIP RESIST	
26	ANISOTROPIC ETCH	Etch silicon mesas
27	SILOX - UNDOPED	SILOX on backs to protect nitride
28	OXIDATION	Grow LOCOS planarizing oxide
29	WET ETCH - NITRIDE	Strip nitride from fronts
30	WET ETCH - OXIDE	Wet etch of screen oxide
31	OXIDATION	Grow field oxide
32	DSW - ACTIVE	Mask to define active regions
33	WET ETCH - OXIDE	Etch oxide from active areas
34	STRIP RESIST	
35	OXIDATION	Grow gate oxide
36	LPCVD - POLY	Deposit poly for gates
37	E-BEAM LITHOGRAPHY	Gate pattern on selected wafers
38	SPLIT RUN	Split - diffused and implanted poly
39	PHOS DIFFUSE	Dope poly on selected wafers
40	E-BEAM LITHOGRAPHY	Gate pattern on remaining wafers
41	RIE - DOPED POLY	Reactive ion etch gates
42	STRIP RESIST	Ash negative e-beam resist
43	OXIDATION	Oxidize poly edges
44	DSW - NPLUS_SD_AS	Open S/D regions for close n-type S/D
45	WET ETCH - OXIDE	Prepare for close n-type S/D implant
46	IMPLANT - As CLOSE	Close n-type S/D into bare silicon
47	IMPLANT - PHOS CLOSE	Close n-type S/D into bare silicon
48	STRIP RESIST	
49	DSW - PPLUS_SD_B	Open S/D regions for close p-type S/D
50	WET ETCH - OXIDE	Prepare for close p-type S/D implant
51	IMPLANT - BORON CLOSE	Close p-type S/D into bare silicon
52	STRIP RESIST	
53	LPCVD - NITRIDE	Deposit nitride for sidewalls
54	RIE - NITRIDE	Etch nitride to form sidewalls
55	DSW - NPLUS_SD_AS	Open n+ regions
56	WET ETCH - OXIDE	Prepare for spaced n+ S/D implant
57	IMPLANT - As SPACED	Implant spaced n+ As S/D
58	IMPLANT - PHOS SPACED	Implant spaced n+ phosphorus S/D
59	STRIP RESIST	
60	DSW - PPLUS_SD_B	Open p+ regions
61	WET ETCH - OXIDE	Prepare for spaced p+ S/D implant
62	IMPLANT - BORON SPACED	Implant spaced p+ boron S/D
63	STRIP RESIST	
64	ANNEAL - NITROGEN	Anneal implants
65	WET ETCH - OXIDE	Prepare for titanium

Continued

Table A.1 -- (Continued)

	STEP	DESCRIPTION
66	METAL EVAPORATION	Titanium for salicide on bare silicon
67	RTA - LOW TEMPERATURE	Form silicides
68	WET ETCH - TITANIUM	Strip excess titanium
69	RTA - HIGH TEMPERATURE	Anneal silicide
70	ANNEAL - FORMING GAS	Forming-gas surface state anneal
71	E-BEAM LITHOGRAPHY	Metalized gate pattern
72	401 METAL EVAPORATION	Ion mill and evaporate Cr-Pd
73	METAL EVAPORATION	Gold to complete gate metal
74	REJECT	Form metalized gates
75	DSW REVERSE - METAL 1	Metal 1 pattern by image reversal
76	401 METAL EVAPORATION	Ion mill and evaporate Cr-Pd
77	METAL EVAPORATION	Gold to complete metal 1
78	REJECT	Form metal 1
79	STOP/CHECK	Measure test patterns
80	DSW - POST	Post pattern in thick resist
81	401 METAL SPUTTER	Backsputter clean and sputter Ti-Au
82	DSW - BRIDGE	Air-bridge pattern
83	GOLD PLATE	Plate air-bridges
84	STRIP RESIST	Flood expose and develop
85	WET ETCH - PLATING BASE	Strip Au-Ti
86	STRIP RESIST	Acetone
87	TEST	DC and RF transistor tests

Table A.2 -- SUMMARY OF MICROX NMOS CIRCUIT PROCESSING SEQUENCE

	STEP		DESCRIPTION
1	MASK DESCRIPTION		
2	TEST PIECES		Select test pieces
3	WAFER SPLITS		Describe wafer splits
4	MARK WAFER ID		
5	SPIN/EXP/DEV	E-BEAM ALIGNER	E-beam zero level alignment marks
6	REACT. ION ETCH	SILICON	RIE silicon, E-beam align. marks
7	ETCH	WET ETCH	Buried oxide
8	STRIP	NEGATIVE RESIST	Strip PMMA
9	SPIN/EXP/DEV	DSW ALIGNER	DSW zero level
10	REACT. ION ETCH	SILICON	RIE DSW zero level
11	ETCH	WET ETCH	Buried oxide

Continued

Table A.2 -- (Continued)

	STEP		DESCRIPTION
12	STRIP	POSITIVE RESIST	Strip resist
13	THERMAL	VIRGIN	Pad oxide
14	LPCVD	SILICON NITRIDE	Nitride over mesa
15	SPIN/EXP/DEV	DSW ALIGNER	Mesa mask
16	REACT. ION ETCH	SILICON NITRIDE	RIE nitride outside mesa
17	STRIP	POSITIVE RESIST	Strip resist
18	THERMAL	VIRGIN	LOCOS oxidation
19	ETCH	WET ETCH	Oxide
20	REACT. ION ETCH	SILICON NITRIDE	Remove nitride from mesa
21	ETCH	WET ETCH	Oxide to planarize
22	THERMAL	VIRGIN	Field oxide
23	IMPLANT	BORON	Blanket channel implant
24	OPEN TUBE		Anneal the implant
25	SPIN/EXP/DEV	DSW ALIGNER	Active mask
26	ETCH	WET ETCH	Oxide in the active area
27	STRIP	POSITIVE RESIST	Strip resist
28	THERMAL	VIRGIN	Gate oxidation
29	LPCVD	POLYSILICON	Gate poly deposition
30	PRE-DEPOSITION	N-TYPE PHOS	Dope poly
31	SPIN/EXP/DEV	E-BEAM ALIGNER	Gates
32	REACT. ION ETCH	POLY-SILICON	RIE poly gates
33	STRIP	POSITIVE RESIST	Strip positive PMMA
34	THERMAL	PRIOR DIFFUSION	Oxidize poly edges
35	IMPLANT	ARSENIC	LDD implant
36	LPCVD	SILICON NITRIDE	Nitride for sidewalls
37	REACT. ION ETCH	SILICON NITRIDE	RIE nitride, form sidewalls
38	ETCH	WET ETCH	BHF etch of oxide in S/D
39	IMPLANT	ARSENIC	S/D n+ implant
40	OPEN TUBE		Anneal the implants
41	ETCH	WET ETCH	Oxide from S/D
42	EVAPORATION	E-BEAM	Titanium for salicide
43	RTA		RTA in forming gas
44	ETCH	WET ETCH	Titanium
45	RTA		RTA in forming gas
46	OPEN TUBE		Forming gas anneal
47	SPIN/EXP/DEV	E-BEAM ALIGNER	E-beam for gate metal
48	SPUTTER		Ion mill, then sputter Cr/Pd
49	EVAPORATION	E-BEAM	Evaporate gold to finish
50	REJECTION		Reject gate metal
51	SPIN/EXP/DEV	DSW ALIGNER	Mask, nichrome resistors
52	EVAPORATION	E-BEAM	Evaporate NiCr

Continued

Table A.2 -- (Continued)

	STEP		DESCRIPTION
53	REJECTION		Reject nichrome
54	HOLD		Hold
55	SPIN/EXP/DEV	DSW ALIGNER	DSW reverse Metal-1 mask
56	EVAPORATION		Ion mill, evap. Cr/Pd 200 A/500 A
57	EVAPORATION	E-BEAM	Evaporate 3500 A Au
58	REJECTION		Reject Metal-1
59	SPIN/EXP/DEV	DSW ALIGNER	Capacitor bottom plate
60	EVAPORATION	E-BEAM	Evaporate 300 A Cr
61	PECVD		Nitride (2600 A) cap diel.
62	REJECTION		Reject Cr and nitride
63	SPIN/EXP/DEV	DSW ALIGNER	8500 post mask
64	SPUTTER		Ti/Au (500 A/500 A), plate base.
65	SPIN/EXP/DEV	DSW ALIGNER	8500 bridge mask
66	PLATE GOLD		Electroplate airbridges (5 μm)
67	STRIP	POSITIVE RESIST	Expose and develop
68	ETCH	WET ETCH	Etch Au/Ti plating base
69	STRIP	POSITIVE RESIST	Post resist strip
70	ENG'R STOP CHECK		RF tests
71	RESIST		Apply protective resist
72	MOUNT WAFERS		Mount wafers for thinning
73	THIN WAFERS		Lap to 100 microns
74	POLISH		Polish lapped surface
75	SPIN/EXP/DEV	CONTACT ALIGNER	IR aligner: Mask-15: via
76	EVAPORATION	E-BEAM	Evap. 5000 A Al, RIE mask
77	REJECTION		Lift off Al
78	SPIN/EXP/DEV	CONTACT ALIGNER	IR aligner: Mask-12C: via
79	ETCH	WET ETCH	Etch Al via pattern
80	STRIP	POSITIVE RESIST	Remove resist from Al
81	REACT. ION ETCH	SILICON	RIE vias to buried oxide
82	ENG'R STOP CHECK		Inspect vias
83	ETCH	WET ETCH	Remove all Al
84	REACT. ION ETCH	SILICON DIOXIDE	RIE oxide inside vias
85	ENG'R STOP CHECK		Inspect vias
86	REACT. ION ETCH	CHROME OXIDE	Etch Cr oxide/Pd to expose Au
87	ENG'R STOP CHECK		Inspect vias
88	SPUTTER		Ti/Au as plating base
89	PLATE GOLD		Electroplate vias, backplane
90	DEMOUNT		Demount wafer from carrier
91	STRIP	WAX AND RESIST	Strip wax, resist from top
92	ENG'R STOP CHECK		Inspect circuits
93	RF TEST		FET and circuit tests

APPENDIX B
SIMULATION OF MICROX FET I-V BEHAVIOR

MICROX FET electrical parameters were modeled using software from Technology Modeling Associates. Examples of input listings for the programs and typical graphical results are given in this appendix.

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***                  TSUPREM-4 (TM)                    ***
***         Version 5.1.0, System H (HP: HP-UX)        ***
***        Copyright (C) 1988, 1989, 1990, 1991        ***
***        Technology Modeling Associates, Inc.        ***
***                All Rights Reserved                 ***
**********************************************************

                    22-Jan-93 11:15:33


 Entering source file nmos.in.

$ MICROX structure

$ X mesh
line    x   location=0      spacing=0.25     tag=left
line    x   location=2.4    spacing=0.025
line    x   location=2.6    spacing=0.025
line    x   location=2.75   spacing=0.05      tag=right

$ Y mesh
line    y   location=0      spacing=0.02     tag=oxtop
line    y   location=0.385  spacing=0.15     tag=oxbottom
line    y   location=2.0    spacing=1.0      tag=sibottom

eliminate columns x.min=2.35 x.max=2.65 y.min=0.05
eliminate columns y.min=0.385

$ define buried oxide and silicon substrate
region    oxide   xlo=left  xhi=right  ylo=oxtop    yhi=oxbottom
region    silicon xlo=left  xhi=right  ylo=oxbottom yhi=sibottom
initialize <100> boron=1e12
   37 lines in the x direction.
   12 lines in the y direction.

$deposit epi with nonuniform vertical grid spacing
deposit   silicon  boron=1e12  thickness=0.08 spaces=8 dy=0.005 ydy=0.08
deposit   silicon  boron=1e12  thickness=0.08 spaces=8 dy=0.005

option device=X
plot.2d  grid

   Top of the device is at y=-0.160 microns.
   Top axis is at y=-0.376 microns.

$stop

$plot initial mesh
option dev=X
select    z=1  title="Initial Mesh"
plot.2d  grid  y.max=1 c.grid=2

   Top of the device is at y=-0.160 microns.
   Top axis is at y=-0.276 microns.
```

```
print.1d x.value=0.0 layers

 Num       Material        Top       Bottom   Thickness        Integral
   1        silicon     -0.1600       0.0000      0.1600       1.6000e-05
              oxide      0.0000       0.3850      0.3850       3.8500e-05
   3        silicon     0.3850       2.0000      1.6150       1.6150e-04


$use vertical oxidation model to grow pad oxide
method   vertical  grid.oxi=4
diffusion  time=4  temp=900  inert
diffusion  time=15 temp=900  weto2
diffusion  time=5  temp=900  inert
print.1d x.value=0.0 layers

 Num       Material        Top       Bottom   Thickness        Integral
   1          oxide     -0.1824      -0.1439      0.0385       3.8513e-06
   2        silicon     -0.1439       0.0000      0.1439       1.4393e-05
   3          oxide      0.0000       0.3850      0.3850       3.8500e-05
   4        silicon      0.3850       1.0051      0.6201       4.7794e-05
   5        silicon      1.0051       1.0051      0.0000       0.0000e+00
   6        silicon      1.0051       2.0000      0.9949       7.9071e-05


$locos oxidation
diffusion  time=75 temp=1000  inert

$etch pad oxide
etch oxide all

$   w field oxide
diffusion  time=4  temp=900  inert
diffusion  time=16 temp=900  weto2
diffusion  time=5  temp=900  inert
print.1d x.value=0.0 layers

 Num       Material        Top       Bottom   Thickness        Integral
   1          oxide     -0.1678      -0.1268      0.0410       4.0959e-06
   2        silicon     -0.1268       0.0000      0.1268       1.2679e-05
   3          oxide      0.0000       0.3850      0.3850       3.8500e-05
   4        silicon      0.3850       2.0000      1.6150       1.6150e-04


$channel implant n-channel p well
implant BF2 dose=4e12 energy=120
option dev=postscript plot.out="dop1"
$option dev=X
select     Z=log10(active(boron)) Title="Doping Profiles"  +
           label="log(Concentration)"
plot.1d    x.value=2.75 bottom=15 top=21 left=-0.15 right=0 line.typ=5 +
           color=2
label      label="Channel Boron (x=2.75)"  x=-.085 y=17.2
select     Z=log10(doping)
plot.1d    x.value=2.75 ^axis ^clear line.typ=2 color=3
label      label="Channel Boron (x=2.75)"  x=-.085 y=17.2

$   annel implant p-channel p- well
$implant BF2 dose=1.5e12 energy=90

$anneal implants
```

```
diffusion  time=20 temp=900 inert

$etch field oxide
etch oxide all

$sacrificial oxide
$diffusion  time=10 temp=900  inert
$diffusion  time=37 temp=900  weto2
$diffusion  time=5  temp=900  inert
$print.1d x.value=0.0 layers

$etch sacrificial oxide
$etch oxide all

$gate oxidation dry
diffusion  time=10 temp=900 inert
diffusion  time=27 temp=900 dryo2
diffusion  time=5  temp=900 inert
diffusion  time=60 temp=1000 inert
print.1d x.value=0.0 layers

 Num      Material       Top      Bottom  Thickness        Integral
   1         oxide   -0.1345    -0.1223     0.0123      2.1467e-05
   2       silicon   -0.1223     0.0000     0.1223      1.8717e-04
   3         oxide    0.0000     0.3850     0.3850      5.7503e-04
   4       silicon    0.3850     2.0000     1.6150      2.3201e-03


$poly deposition and n+ doping
deposit  poly thick=0.3  spaces=6
d   use  time=33 temp=950 phos=1e21
etch poly left p1.x=2.6

$oxidize poly
diffusion  time=10 temp=1000 inert
diffusion  time=18 temp=1000 dryo2
diffusion  time=5  temp=1000 inert

$LDD implant n-channel
implant  As dose=6e12 energy=110
$implant  As dose=9e12 energy=80
option dev=postscript plot.out="dop2"
select     Z=log10(active(arsenic)) Title="Doping Profiles"  +
           label="log(Concentration)"
plot.1d    x.value=2.5 bottom=15 top=21 left=-0.15 right=0 line.typ=5 +
           color=2
label      label="LDD Arsenic (x=2.5)"  x=-.085 y=18.2
select     Z=log10(doping)
plot.1d    x.value=2.5 ^axis ^clear line.typ=2 color=3

$LDD implant p-channel
$implant  BF2 dose=6e12 energy=94


$nitride deposition and definition
deposit  nitride thick=0.2 spaces=2
d   use  time=54 temp=800 inert
savefile out.file=tempfile
$
select    z=doping title="MICROX n-channel FET"
```

```
option dev=X
plot.2d  y.max=1

   Top of the device is at y=-0.644 microns.
    op axis is at y=-0.808 microns.

color    silicon  color=7
color    oxide    color=5
color    poly     color=3
color    nitride  color=4
color    aluminum color=2
foreach  X ( 16 to 21 step 1 )
  contour  value=( 10^ 16 )   color=4 line.typ=2
  contour  value=(-(10^ 16 ))   color=2 line.typ=5
  contour  value=( 10^ 17 )   color=4 line.typ=2
  contour  value=(-(10^ 17 ))   color=2 line.typ=5
  contour  value=( 10^ 18 )   color=4 line.typ=2
  contour  value=(-(10^ 18 ))   color=2 line.typ=5
  contour  value=( 10^ 19 )   color=4 line.typ=2
  contour  value=(-(10^ 19 ))   color=2 line.typ=5
  contour  value=( 10^ 20 )   color=4 line.typ=2
  contour  value=(-(10^ 20 ))   color=2 line.typ=5
  contour  value=( 10^ 21 )   color=4 line.typ=2
  contour  value=(-(10^ 21 ))   color=2 line.typ=5
end
plot.2d  ^ax  ^cl
$
etch     nitride old.dry thicknes=0.2
select   z=doping  title="MICROX n-channel FET"
$option dev=ps plot.out="ps2"
p.   .2d  y.max=1

   Top of the device is at y=-0.444 microns.
   Top axis is at y=-0.588 microns.

color    silicon  color=7
color    oxide    color=5
color    poly     color=3
color    nitride  color=4
color    aluminum color=2
foreach  x ( 16 to 21 step 1 )
  contour  value=( 10^ 16 )     color=4 line.typ=2
  contour  value=(-(10^ 16 ))  color=2 line.typ=5
  contour  value=( 10^ 17 )     color=4 line.typ=2
  contour  value=(-(10^ 17 ))  color=2 line.typ=5
  contour  value=( 10^ 18 )     color=4 line.typ=2
  contour  value=(-(10^ 18 ))  color=2 line.typ=5
  contour  value=( 10^ 19 )     color=4 line.typ=2
  contour  value=(-(10^ 19 ))  color=2 line.typ=5
  contour  value=( 10^ 20 )     color=4 line.typ=2
  contour  value=(-(10^ 20 ))  color=2 line.typ=5
  contour  value=( 10^ 21 )     color=4 line.typ=2
  contour  value=(-(10^ 21 ))  color=2 line.typ=5
end
plot.2d  ^ax  ^cl
$

$strip oxide from S/D and poly
etch oxide old.dry thicknes=0.05
$
```

```
select   z=doping  title="MICROX n-channel FET"
$option dev=ps plot.out="ps3"
plot.2d  y.max=1

    op of the device is at y=-0.444 microns.
   Top axis is at y=-0.588 microns.

color    silicon  color=7
color    oxide    color=5
color    poly     color=3
color    nitride  color=4
color    aluminum color=2
foreach  x ( 16 to 21 step 1 )
  contour  value=( 10^ 16 )     color=4 line.typ=2
  contour  value=(-(10^ 16 ))  color=2 line.typ=5
  contour  value=( 10^ 17 )     color=4 line.typ=2
  contour  value=(-(10^ 17 ))  color=2 line.typ=5
  contour  value=( 10^ 18 )     color=4 line.typ=2
  contour  value=(-(10^ 18 ))  color=2 line.typ=5
  contour  value=( 10^ 19 )     color=4 line.typ=2
  contour  value=(-(10^ 19 ))  color=2 line.typ=5
  contour  value=( 10^ 20 )     color=4 line.typ=2
  contour  value=(-(10^ 20 ))  color=2 line.typ=5
  contour  value=( 10^ 21 )     color=4 line.typ=2
  contour  value=(-(10^ 21 ))  color=2 line.typ=5
end
plot.2d  ^ax  ^cl
$

savefile  out.file=midstream
$S   implant n-channel
implant  As dose=3e15 energy=65

$S/D implant p-channel
$implant  BF2 dose=3e15 energy=94

$S/D anneal
diffusion time=30 temp=850 inert

$metallization
deposit  aluminum  thick=0.3
  deposit  photoresist thick=1.0
etch     photoresist right p1.x=1.7
etch     aluminum trap thick=0.7 angle=85
etch     photoresist all

$reflect structure, then save complete transistor
savefile  out.file=nmosout
structure reflect right
savefile  out.file=nmosout2  medici
Electrode 1: xmin    0.000 xmax    1.665 ymin   -0.115 ymax   -0.115
Electrode 2: xmin    3.835 xmax    5.500 ymin   -0.115 ymax   -0.115

$plot grid and profiles for complete structure
select   z=doping  title="MICROX n-channel FET"
$option dev=ps plot.out="ps4"
plot.2d y.max=1

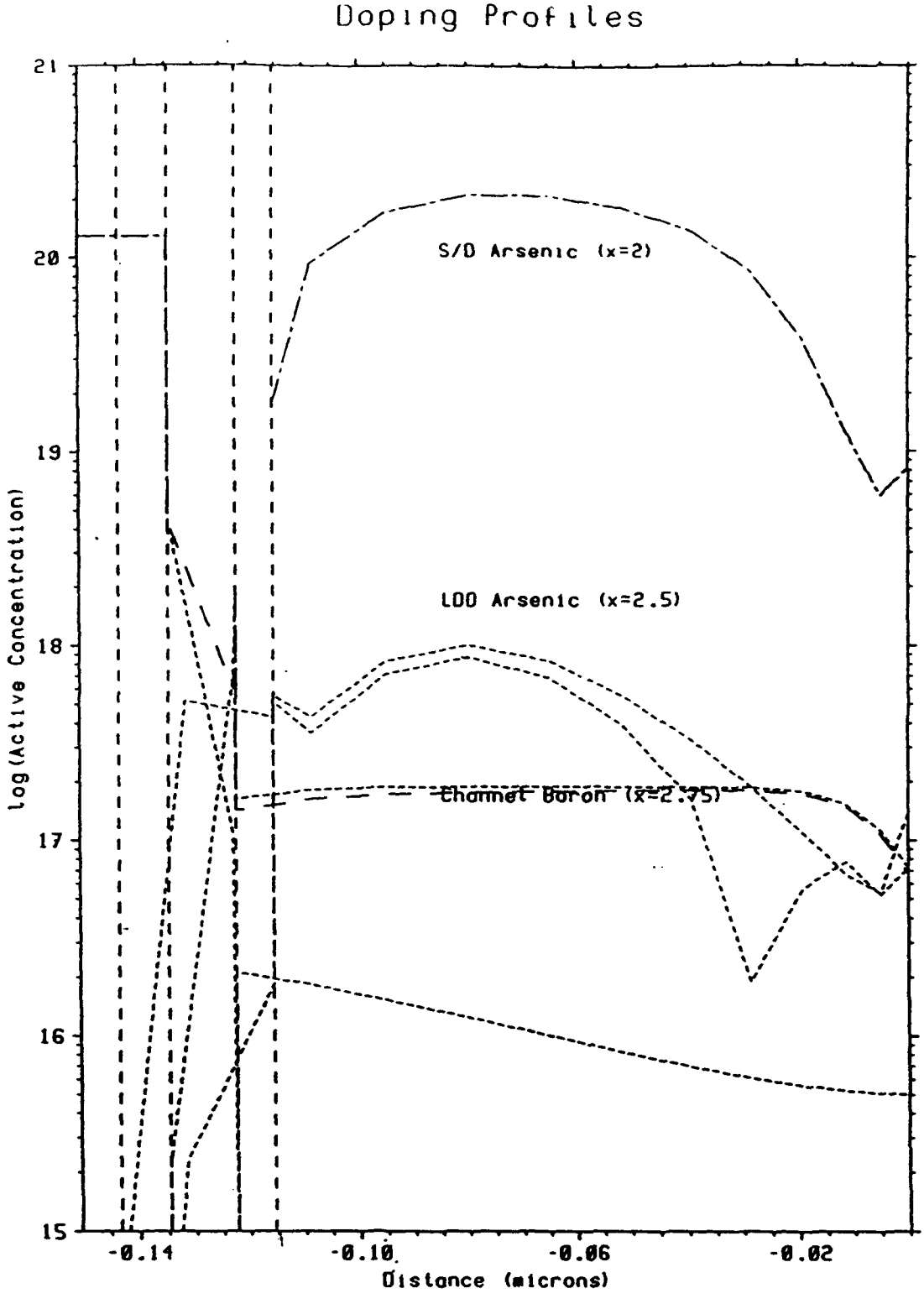
   Top of the device is at y=-0.444 microns.
   Top axis is at y=-0.588 microns.
```

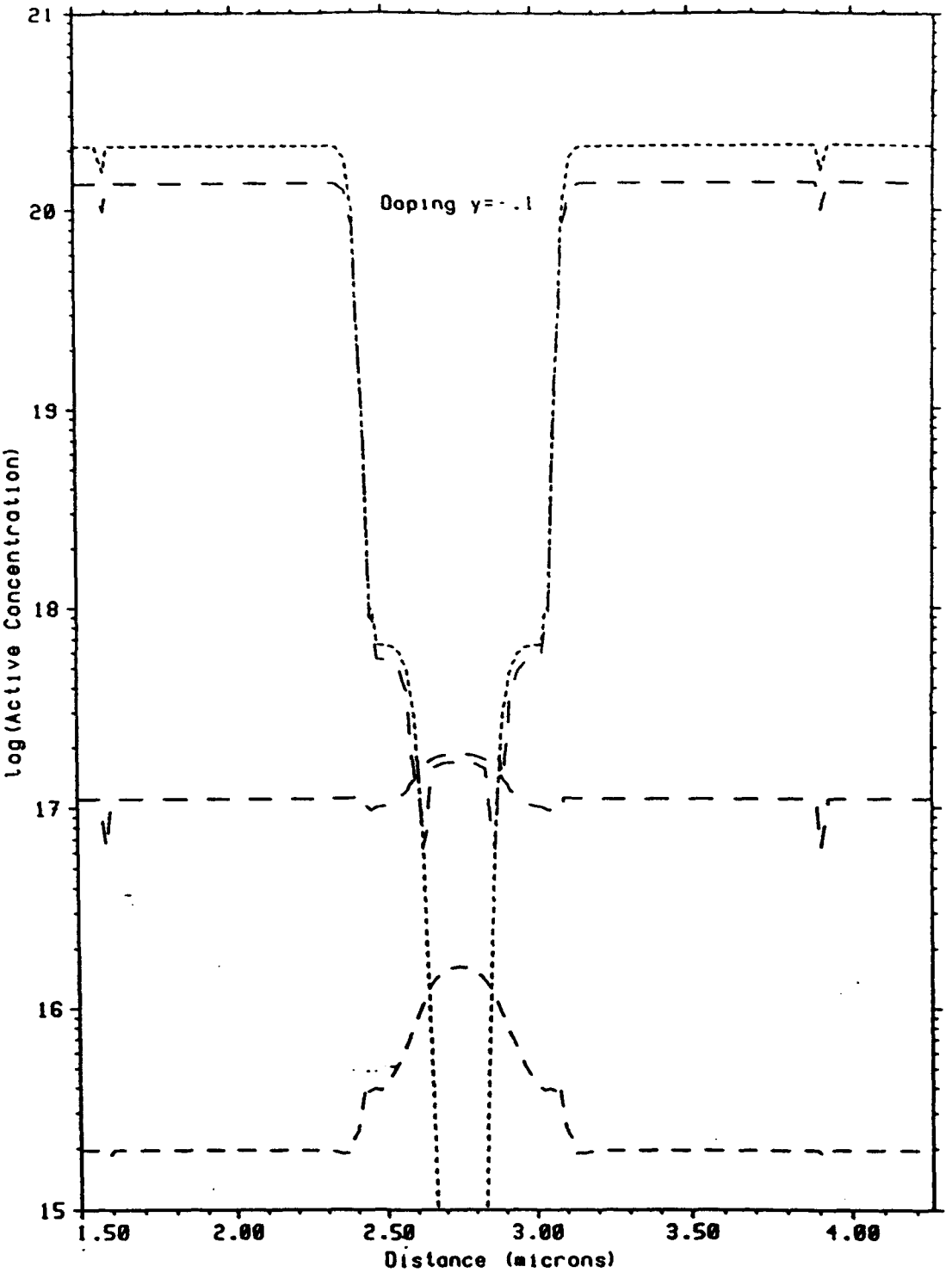
```
color     silicon  color=7
color     oxide    color=5
color     poly     color=3
color     nitride  color=4
color     aluminum color=2
foreach   x ( 16 to 21 step 1 )
  contour  value=( 10^ 16 )      color=4 line.typ=2
  contour  value=(-(10^ 16 ))  color=2 line.typ=5
  contour  value=( 10^ 17 )      color=4 line.typ=2
  contour  value=(-(10^ 17 ))  color=2 line.typ=5
  contour  value=( 10^ 18 )      color=4 line.typ=2
  contour  value=(-(10^ 18 ))  color=2 line.typ=5
  contour  value=( 10^ 19 )      color=4 line.typ=2
  contour  value=(-(10^ 19 ))  color=2 line.typ=5
  contour  value=( 10^ 20 )      color=4 line.typ=2
  contour  value=(-(10^ 20 ))  color=2 line.typ=5
  contour  value=( 10^ 21 )      color=4 line.typ=2
  contour  value=(-(10^ 21 ))  color=2 line.typ=5
end
plot.2d  ^ax  ^cl

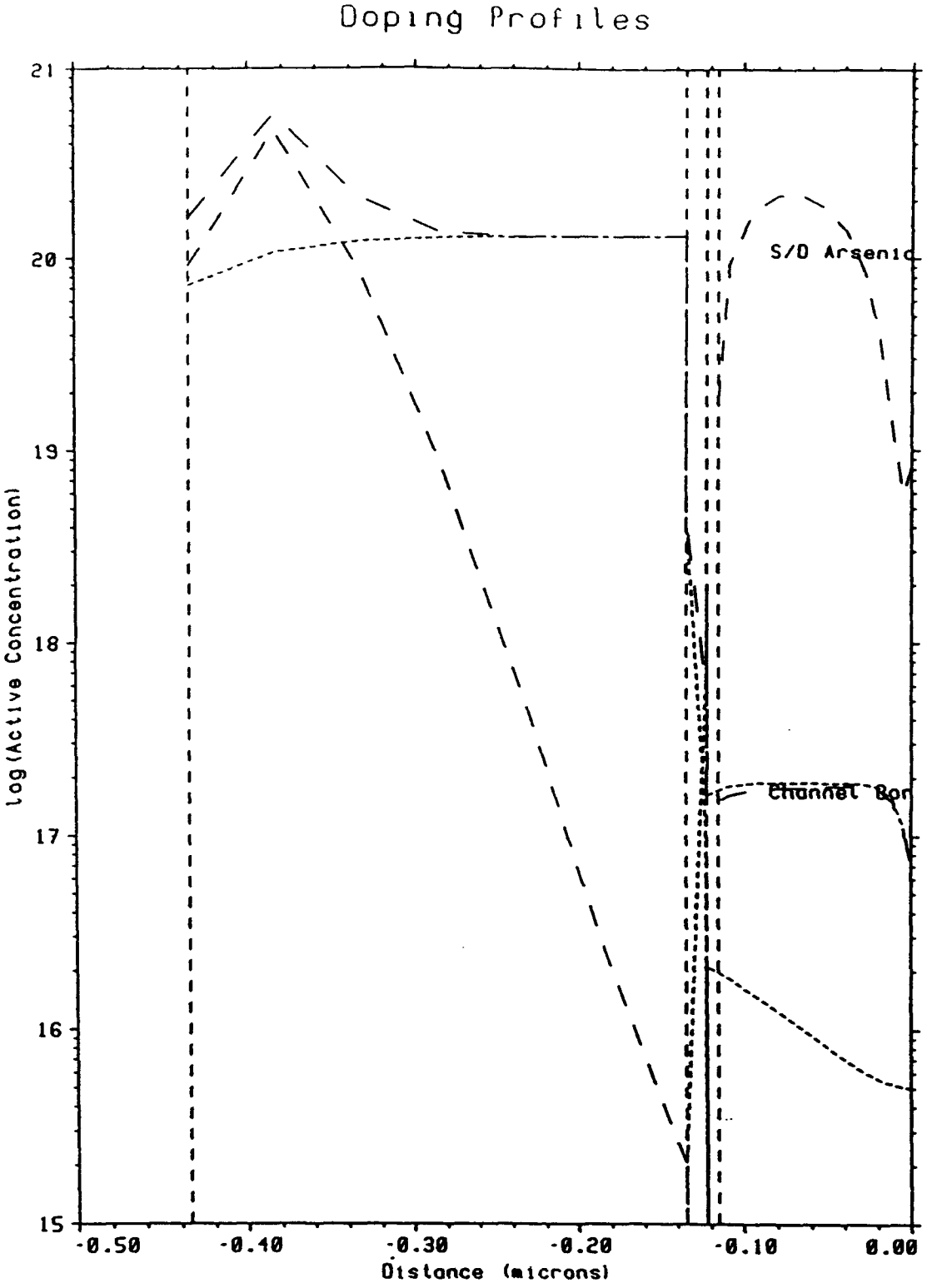
$option dev=ps plot.out="ps5"
$plot.2d grid y.max=1 c.grid=2

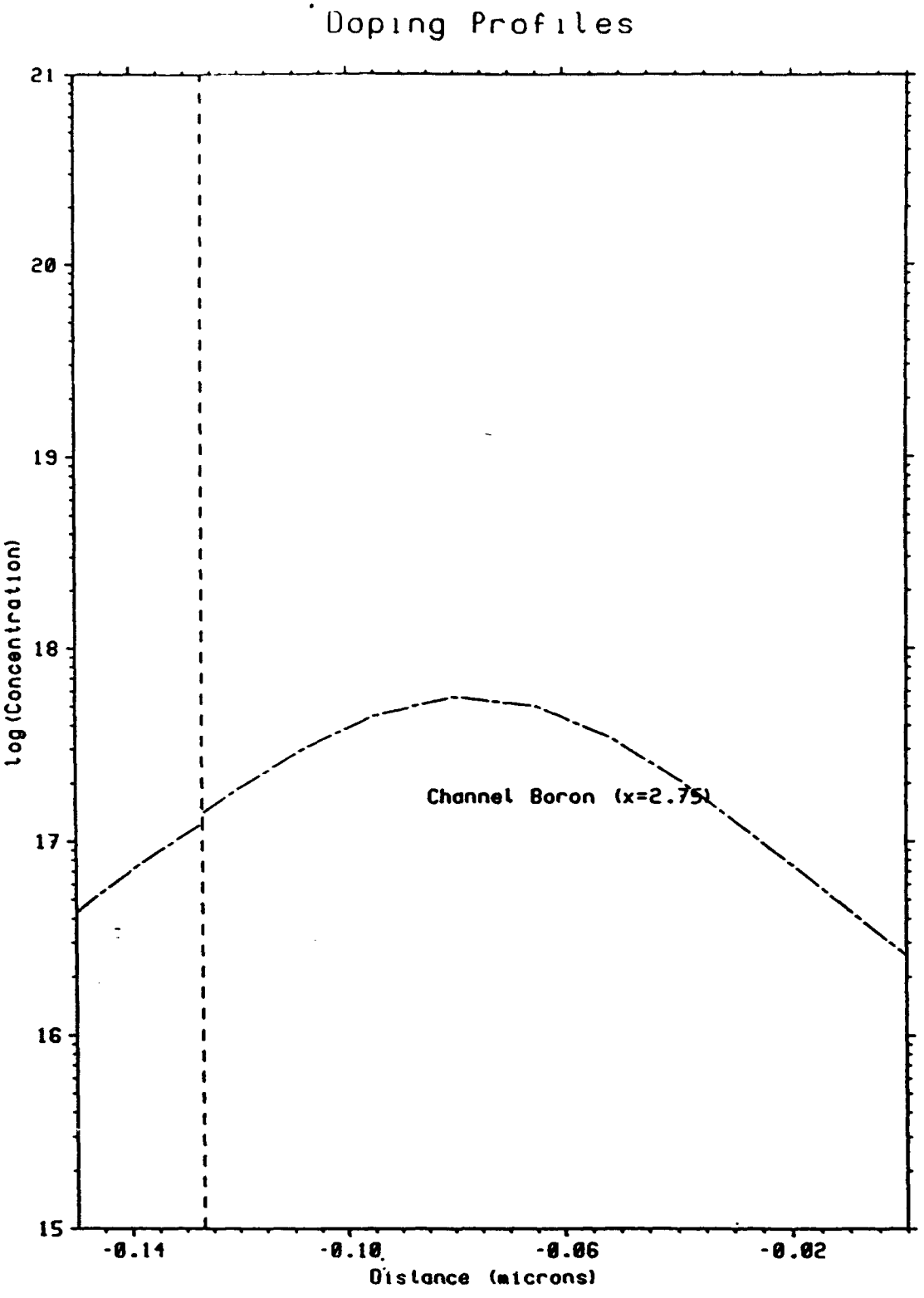

 Exiting source file nmos.in.

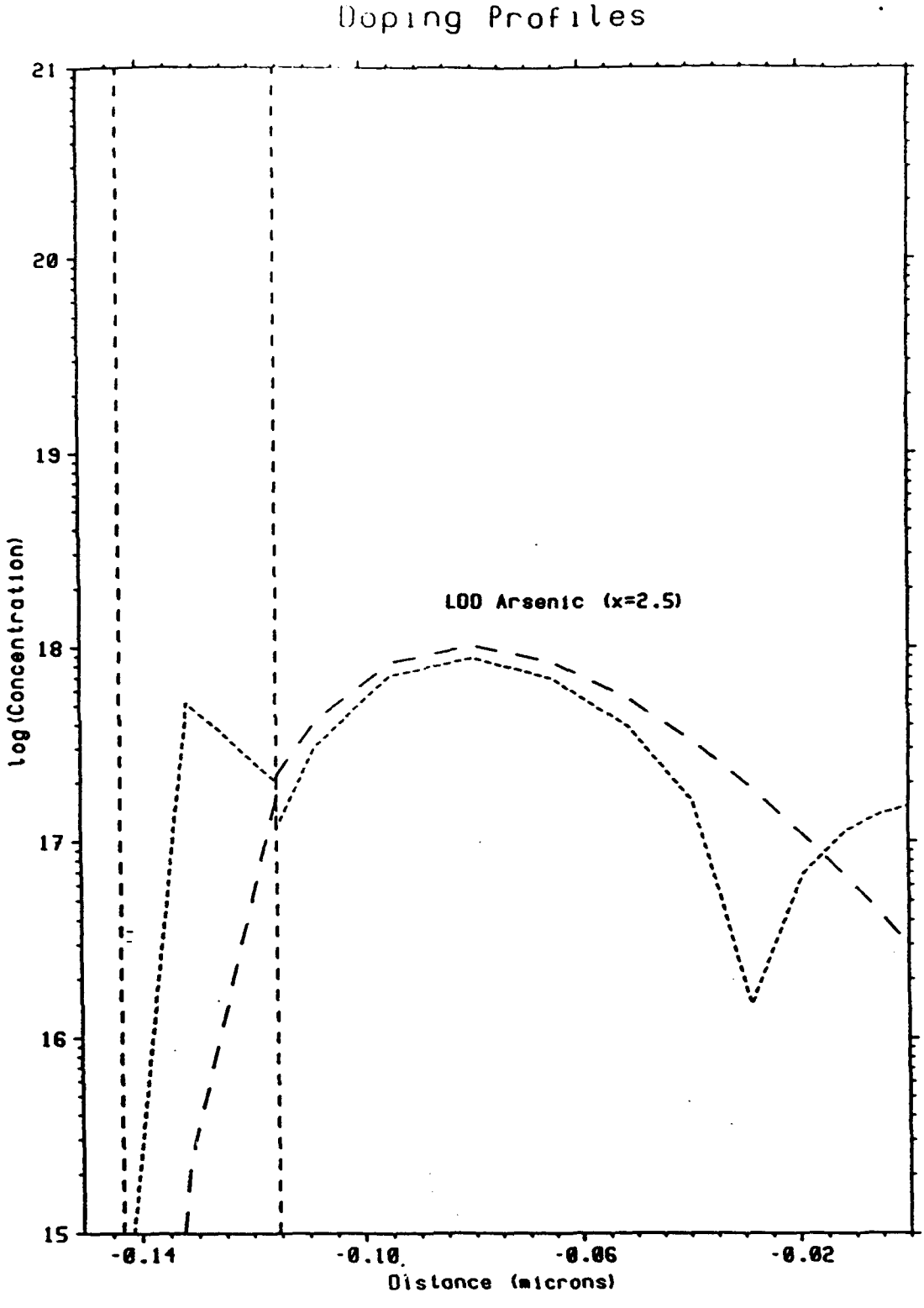

 *** END TSUPREM-4 ***
```

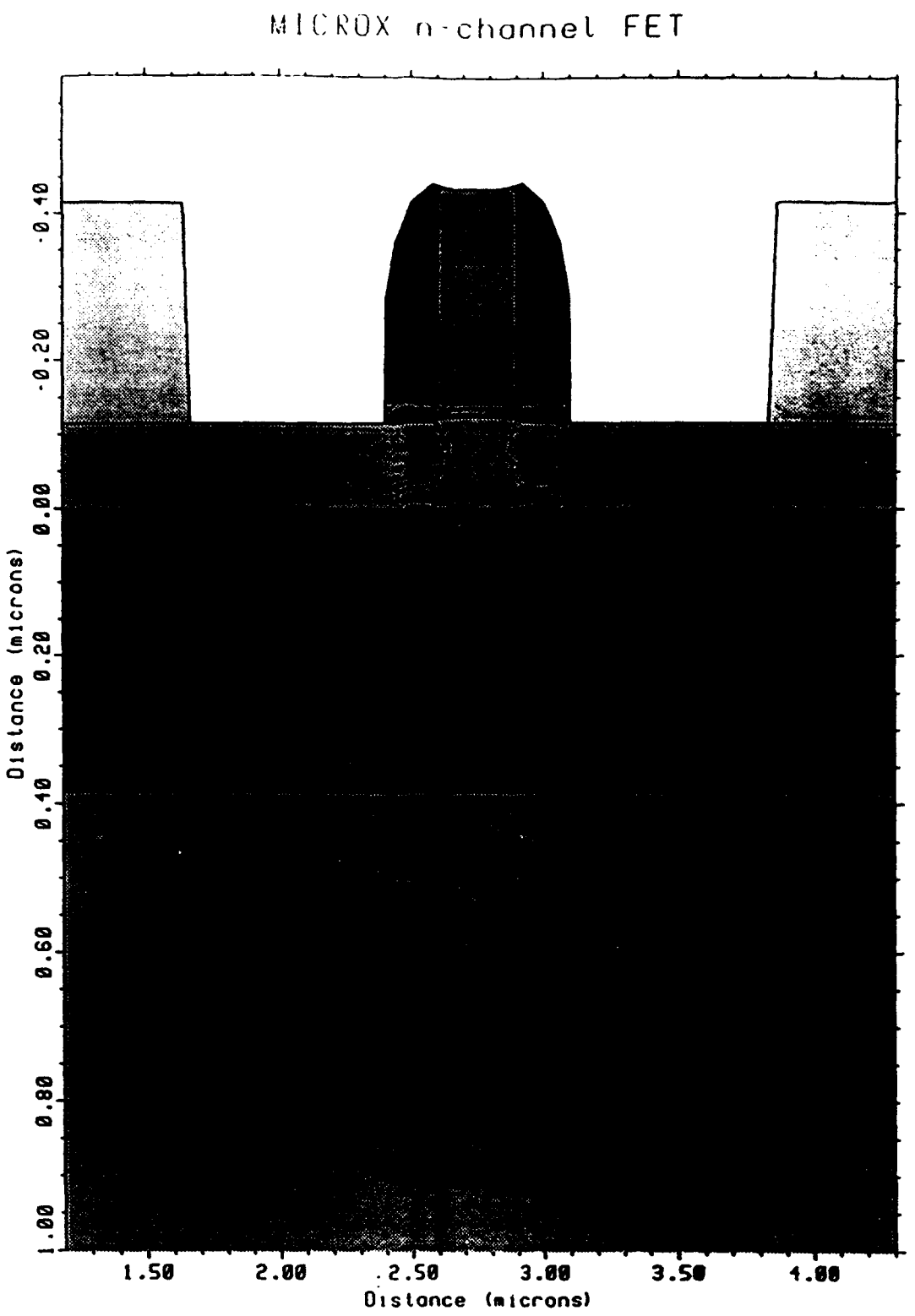

Doping Profiles
21
20
19
18
17
16
15
Log(Active Concentration)
S/D Arsenic (x=2)
LDD Arsenic (x=2.5)
Channel Boron (x=2.75)
-0.14
-0.10
-0.06
-0.02
Distance (microns)

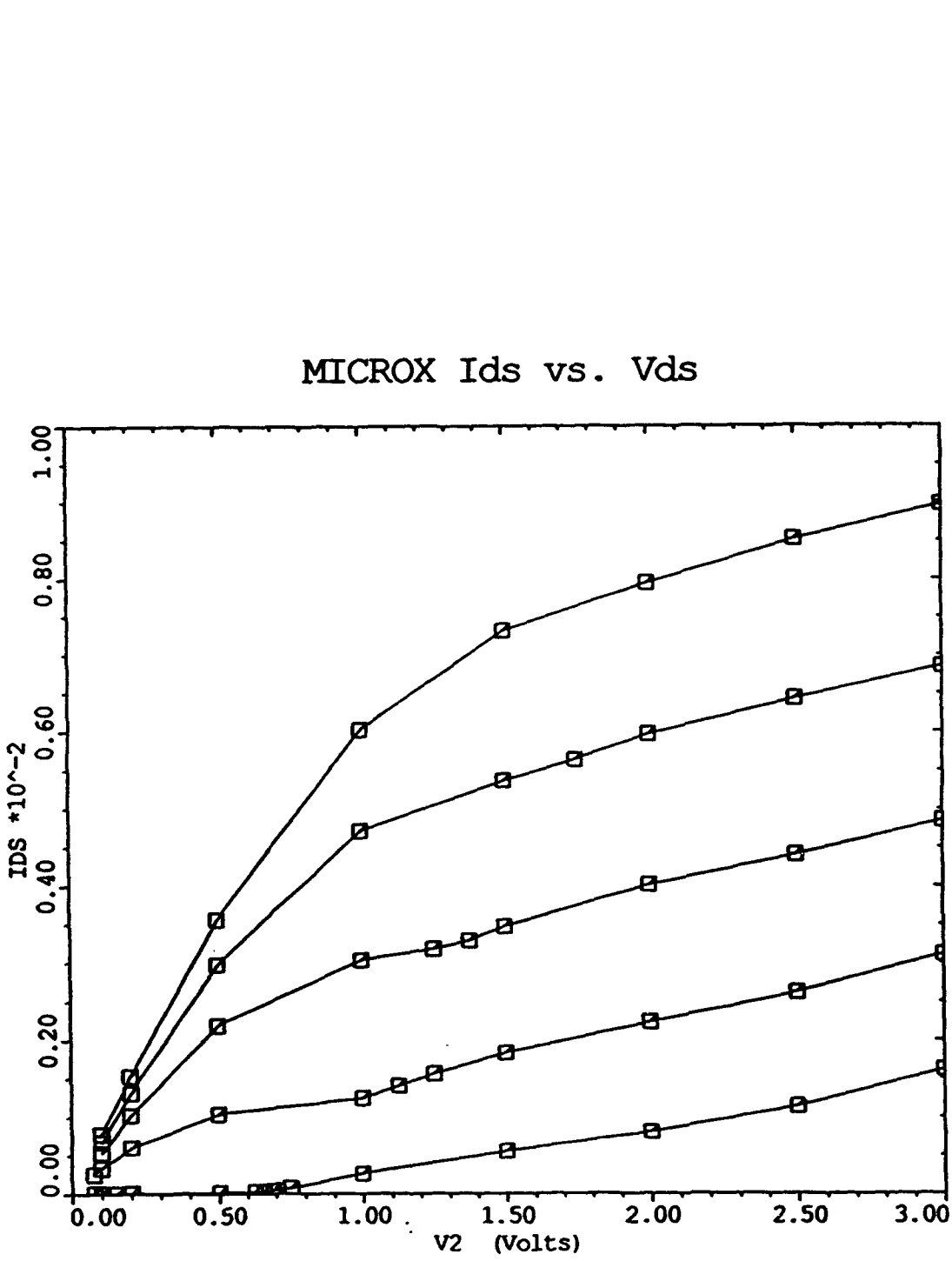

Doping Profiles
Doping y=-.1
log(Active Concentration)
21
20
19
18
17
16
15
1.50
2.00
2.50
3.00
3.50
4.00
Distance (microns)


Doping Profiles
21
20
19
18
17
16
15
Log(Active Concentration)
S/D Arsenic
Channel Bor
-0.50
-0.40
-0.30
-0.20
-0.10
0.00
Distance (microns)


Doping Profiles
21
20
19
18
17
16
15
Log (Concentration)
Channel Boron (x=2.75)
-0.14
-0.10
-0.06
-0.02
Distance (microns)


Doping Profiles
21
20
19
18
17
16
15
log (Concentration)
LDD Arsenic (x=2.5)
-0.14
-0.10
-0.06
-0.02
Distance (microns)


MICROX n-channel FET
-0.40
-0.20
0.00
0.20
0.40
0.60
0.80
1.00
Distance (microns)
1.50
2.00
2.50
3.00
3.50
4.00
Distance (microns)


MICROX Ids vs. Vds
IDS *10^-2
0.00
0.20
0.40
0.60
0.80
1.00
0.00
0.50
1.00
1.50
2.00
2.50
3.00
V2 (Volts)

```
$ MICROX structure

$ X mesh
line    x   location=0      spacing=0.25     tag=left
l       x   location=2.4    spacing=0.025
line    x   location=2.6    spacing=0.025
line    x   location=2.75   spacing=0.05      tag=right

$ Y mesh
line    y   location=0      spacing=0.02     tag=oxtop
line    y   location=0.385  spacing=0.15     tag=oxbottom
line    y   location=2.0    spacing=1.0      tag=sibottom

eliminate columns x.min=2.35 x.max=2.65 y.min=0.05
eliminate columns y.min=0.385

$ define buried oxide and silicon substrate
region    oxide   xlo=left  xhi=right  ylo=oxtop     yhi=oxbottom
region    silicon xlo=left  xhi=right  ylo=oxbottom yhi=sibottom
initialize <100> boron=1e12

$deposit epi with nonuniform vertical grid spacing
deposit   silicon  boron=1e12  thickness=0.08 spaces=8 dy=0.005 ydy=0.08
deposit   silicon  boron=1e12  thickness=0.08 spaces=8 dy=0.005

option device=X
plot.2d  grid
$stop

$plot initial mesh
option dev=X
select    z=1  title="Initial Mesh"
plot.2d  grid  y.max=1 c.grid=2
print.1d x.value=0.0 layers

$use vertical oxidation model to grow pad oxide
method    vertical  grid.oxi=4
diffusion  time=4  temp=900  inert
diffusion  time=15 temp=900  weto2
diffusion  time=5  temp=900  inert
print.1d x.value=0.0 layers

$locos oxidation
diffusion  time=75 temp=1000  inert

$etch pad oxide
etch oxide all

$grow field oxide
diffusion  time=4  temp=900  inert
diffusion  time=16 temp=900  weto2
diffusion  time=5  temp=900  inert
print.1d x.value=0.0 layers

$channel implant n-channel p well
implant BF2 dose=4e12 energy=120
option dev=postscript plot.out="dop1"
$option dev=X
select     Z=log10(active(boron)) Title="Doping Profiles"  +
           label="log(Concentration)"
```

```
plot.1d    x.value=2.75 bottom=15 top=21 left=-0.15 right=0 line.typ=5 +
           color=2
label      label="Channel Boron (x=2.75)"  x=-.085 y=17.2
select     Z=log10(doping)
pl   1d    x.value=2.75 ^axis ^clear line.typ=2 color=3
label      label="Channel Boron (x=2.75)"  x=-.085 y=17.2

$channel implant p-channel p- well
$implant BF2 dose=1.5e12 energy=90

$anneal implants
diffusion  time=20 temp=900 inert

$etch field oxide
etch oxide all

$sacrificial oxide
$diffusion  time=10 temp=900  inert
$diffusion  time=37 temp=900  weto2
$diffusion  time=5  temp=900  inert
$print.1d x.value=0.0 layers

$etch sacrificial oxide
$etch oxide all

$gate oxidation dry
diffusion  time=10 temp=900 inert
diffusion  time=27 temp=900 dryo2
diffusion  time=5  temp=900 inert
diffusion  time=60 temp=1000 inert
pr   .1d x.value=0.0 layers

$poly deposition and n+ doping
deposit  poly thick=0.3  spaces=6
diffuse  time=33 temp=950 phos=1e21
etch poly left p1.x=2.6

$oxidize poly
diffusion  time=10 temp=1000 inert
diffusion  time=18 temp=1000 dryo2
diffusion  time=5  temp=1000 inert

$LDD implant n-channel
implant  As dose=6e12 energy=110
$implant  As dose=9e12 energy=80
option dev=postscript plot.out="dop2"
select     Z=log10(active(arsenic)) Title="Doping Profiles"  +
           label="log(Concentration)"
plot.1d    x.value=2.5 bottom=15 top=21 left=-0.15 right=0 line.typ=5 +
           color=2
label      label="LDD Arsenic (x=2.5)"  x=-.085 y=18.2
select     Z=log10(doping)
plot.1d    x.value=2.5 ^axis ^clear line.typ=2 color=3

$LDD implant p-channel
$implant  BF2 dose=6e12 energy=94


$nitride deposition and definition
deposit  nitride thick=0.2 spaces=2
```

```
diffuse  time=54 temp=800 inert
savefile out.file=tempfile
$
select   z=doping title="MICROX n-channel FET"
op   n dev=X
plot.2d  y.max=1
color    silicon  color=7
color    oxide    color=5
color    poly     color=3
color    nitride  color=4
color    aluminum color=2
foreach  X ( 16 to 21 step 1 )
  contour  value=( 10^ X )   color=4 line.typ=2
  contour  value=(-(10^ X ))   color=2 line.typ=5
end
plot.2d  ^ax  ^cl
$
etch     nitride old.dry thicknes=0.2
select   z=doping  title="MICROX n-channel FET"
$option dev=ps plot.out="ps2"
plot.2d  y.max=1
color    silicon  color=7
color    oxide    color=5
color    poly     color=3
color    nitride  color=4
color    aluminum color=2
foreach  x ( 16 to 21 step 1 )
  contour  value=( 10^ x )     color=4 line.typ=2
  contour  value=(-(10^ x ))  color=2 line.typ=5
end
pl   2d  ^ax  ^cl
$

$strip oxide from S/D and poly
etch oxide old.dry thicknes=0.05
$
select   z=doping  title="MICROX n-channel FET"
$option dev=ps plot.out="ps3"
plot.2d  y.max=1
color    silicon  color=7
color    oxide    color=5
color    poly     color=3
color    nitride  color=4
color    aluminum color=2
foreach  x ( 16 to 21 step 1 )
  contour  value=( 10^ x )     color=4 line.typ=2
  contour  value=(-(10^ x ))  color=2 line.typ=5
end
plot.2d  ^ax  ^cl
$

savefile  out.file=midstream
$S/D implant n-channel
implant  As dose=3e15 energy=65

$S/D implant p-channel
$i   .ant  BF2 dose=3e15 energy=94

$S/D anneal
diffusion time=30 temp=850 inert
```

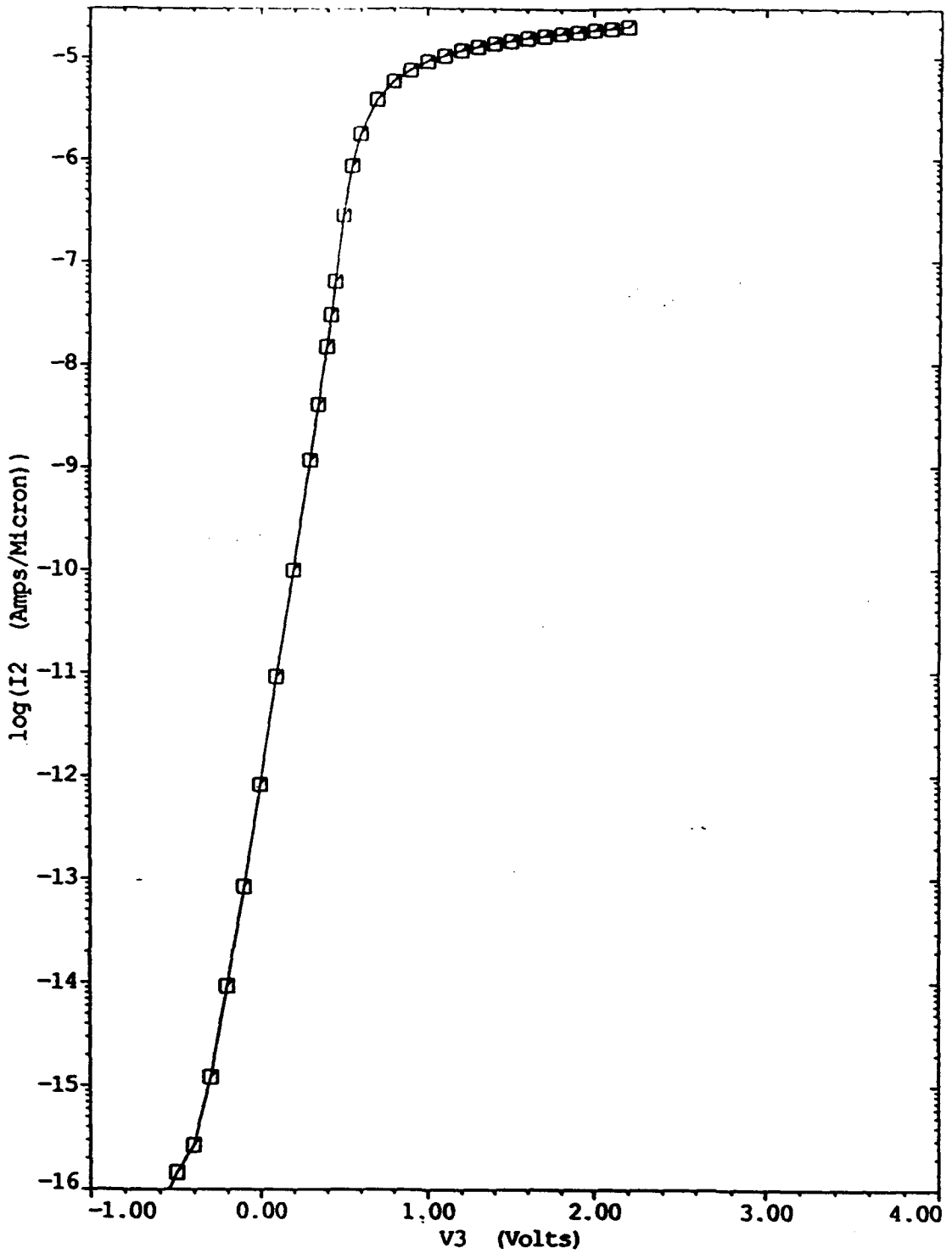
```
$metallization
deposit  aluminum  thick=0.3
  deposit  photoresist thick=1.0
e         photoresist right pl.x=1.7
etch      aluminum trap thick=0.7 angle=85
etch      photoresist all

$reflect structure, then save complete transistor
savefile  out.file=nmosout
structure reflect right
savefile  out.file=nmosout2  medici

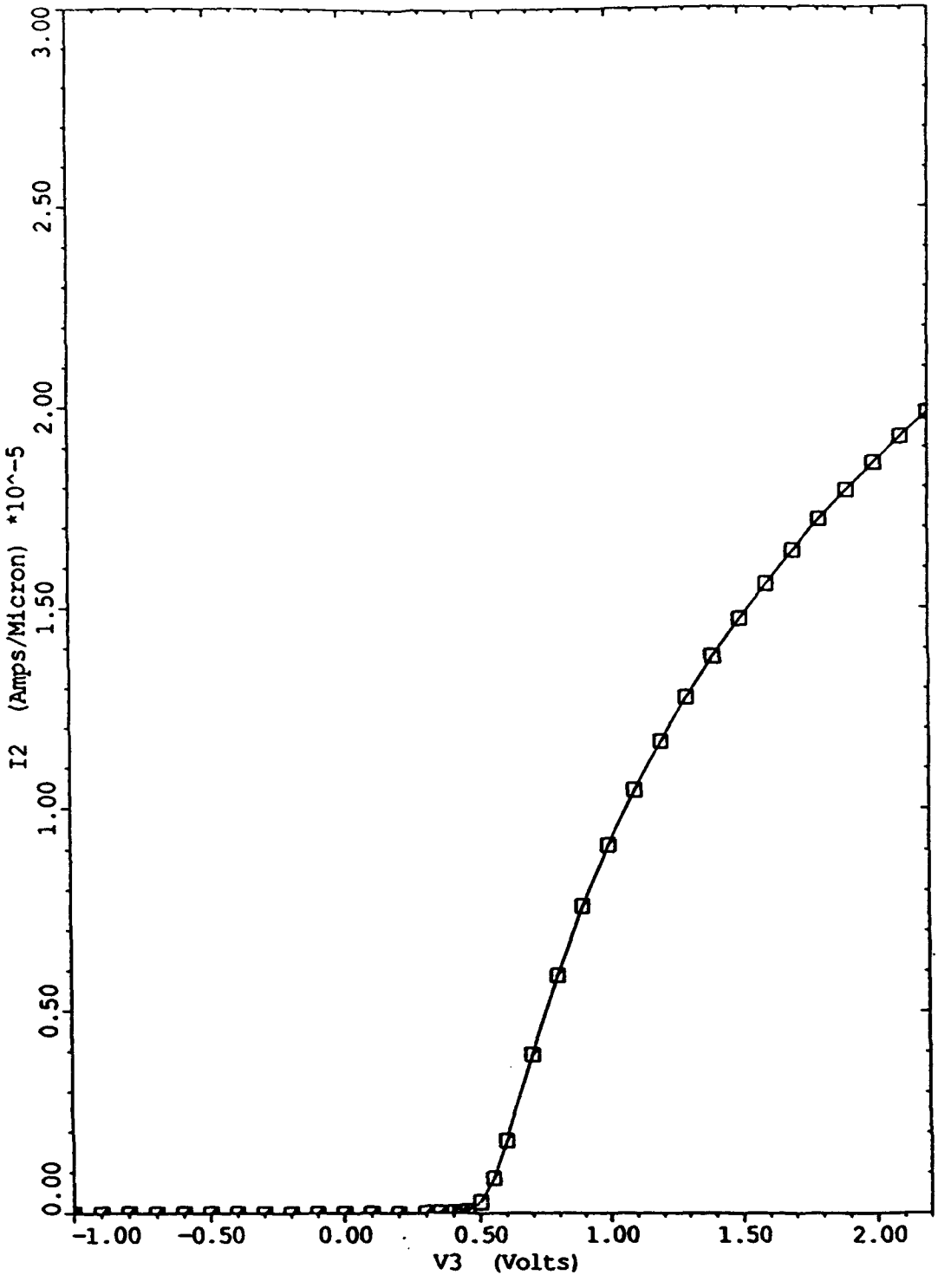
$plot grid and profiles for complete structure
select    z=doping  title="MICROX n-channel FET"
$option dev=ps plot.out="ps4"
plot.2d y.max=1
color     silicon  color=7
color     oxide    color=5
color     poly     color=3
color     nitride  color=4
color     aluminum color=2
foreach  x ( 16 to 21 step 1 )
  contour  value=( 10^ x )     color=4 line.typ=2
  contour  value=(-(10^ x ))  color=2 line.typ=5
end
plot.2d  ^ax  ^cl

$option dev=ps plot.out="ps5"
$plot.2d grid y.max=1 c.grid=2
```

MICROX Ids vs. Vgs



MICROX Ids vs. Vgs



APPENDIX C
MICROX FOR POWER MOS FROM L TO X BAND

The low thermal conductivity (0.0088 W/cm/deg C) of the buried oxide layer, about 1/10 that of silicon, in MICROX introduces an additional thermal impedance, compared to devices of similar structure in bulk silicon substrates. At issue is the effect of this oxide layer contribution in practical device structures. This appendix treats geometric considerations of thermal impedance in typical digital and RF devices.

MICROX™ for Power MOS from L to X Band

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SIMOX technology employs a high energy oxygen implant to form a thin insulating layer of silicon dioxide just below the channel of the MOSFET. A special class of SIMOX technology, known as MICROX™ which uses a high resistivity substrate to reduce parasitics, has resulted in record-setting f_{max} values of 42 GHz. The insulating silicon dioxide layer not only electrically isolates the MOSFET from the bulk of the semiconductor, but also tends to thermally isolate the device because of the low thermal conductivity of oxide compared to silicon. This would appear to limit MICROX™ to non-power applications since the heat generated in a MICROX™ device causes a greater temperature rise than in a bulk device operated at the same bias point. The rise in the local temperature results in reduced carrier mobility, yielding a reduction in drain current, transconductance, and speed.

In studying the effects of heating on device performance, two application areas of MICROX™ technology are considered: digital, where packing densities require close placement of adjacent devices, and microwave power, where monolithic circuits contain large spiral inductors and capacitors which consume most of the area compared with the active elements. In such a microwave circuit, the MOSFET's are 10 to 20 microns apart. Using two-dimensional modeling of a 0.5μm gate length device structure, we have determined the digital case corresponds to a point source of heat resulting in an excessive channel temperature for a power density of 10W/cm. In extreme cases, this may lead to a negative differential resistance region in the output characteristics. However, the microwave device behaves more like a parallel plate heat source in which the heat is allowed to dissipate laterally, and the rise in temperature has little effect on the output characteristics of the device.

The two-dimensional modeling was implemented using the MEDICI software from Technology Modeling Associates. In this software a cross section of the device structure, doping densities, and geometry forms the input. A coupled solution of Poisson's equation, current-continuity equations, and the heat equation is obtained for a bias point. By incrementing the bias point, a sweep of the drain current for a given gate voltage may be obtained.

Results of two calculations are shown in Figures 1 and 2, where the former simulates a device in a high density digital application and the latter simulates a device in a monolithic microwave circuit. Each simulation is run for the same bias conditions. In both cases the buried oxide thickness is 1000Å and the active silicon layer is 1000Å. As seen in Figure 1a., a total

device length of 1.5μm (0.5μm gate length and 0.5μm drain-source lengths) results in a maximum device temperature of 380K for a power density of 10W/cm. By considering 0.5μm drain-source regions for the simulations, we are examining heating effects principally dominated by the effective channel length[1]. A reduction of 10% in the magnitude of the saturated drain current at 10W/cm is also observed in Figure 1b. The lattice temperature for a 0.5μm gate length device is shown in Figure 2a.; however, the simulation is allowed to extend +/-20μm from the channel area. The rise in temperature is only 30K, and from Figure 2b. a much lower degradation in channel current is observed. These two MICROX™ cases and two corresponding ones for non-SOI bulk structures are summarized in Table 1.

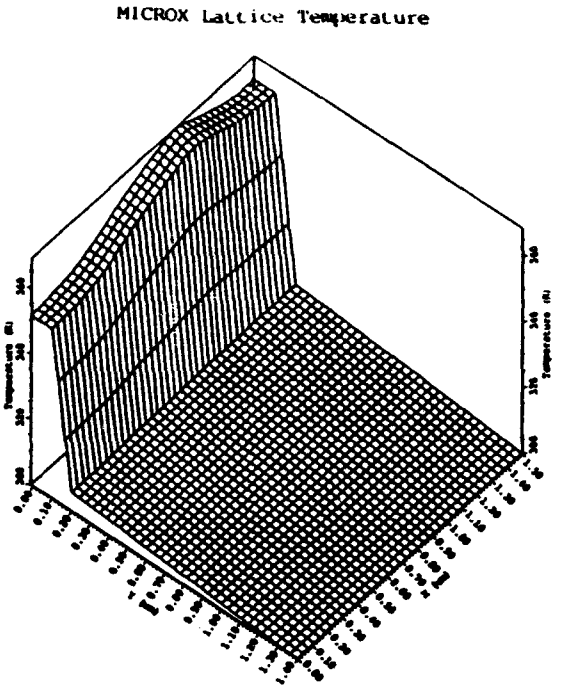
Technology	Simulation Length (μm)	Maximum Temperature Rise (K)
MICROX™	1.5 (digital)	80
MICROX™	40 (power)	30
Bulk	1.5 (digital)	11
Bulk	40 (power)	4.5

Table 1. A comparison between MICROX™ and bulk temperature rise for a 10W/cm power density and total source-drain lengths corresponding to logic and power device applications.

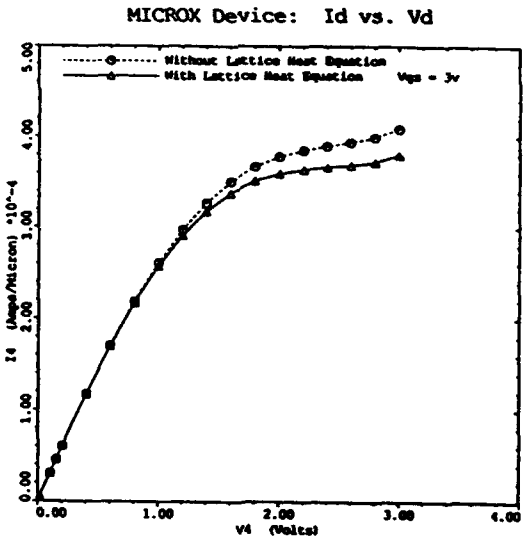
We explored MICROX™ power configurations when the buried oxide is reduced from 1000Å to 500Å. *This lowered the maximum rise in channel temperature to only 18K and produced no degradation in channel current.* In a conventional SIMOX process, thinning the buried oxide to 500Å may result in a reduced electrical isolation by the buried layer due to silicon pipes and other structural defect mechanisms. The effects would not be as severe in the MICROX™ case owing to the high resistivity substrate which inherently isolates the devices.

Even with the low thermal conductivity of the buried oxide in SOI structures, we have demonstrated the feasibility of MICROX™ structures operating at a 10W/cm power dissipation level for device geometries typical of microwave monolithic circuits. MICROX™ technology has a definite advantage over the standard SIMOX process in this regard since the high resistivity substrate, in conjunction with the buried oxide layer, reduces parasitic coupling.

1. L.J. McDaid, S. Hall, P.H. Mellor, and W. Eccleston: "Physical Origin of Negative Differential Resistance in SOI Transistors", *Electronics Letters*, 1989, 25, (13), pp. 827-828.

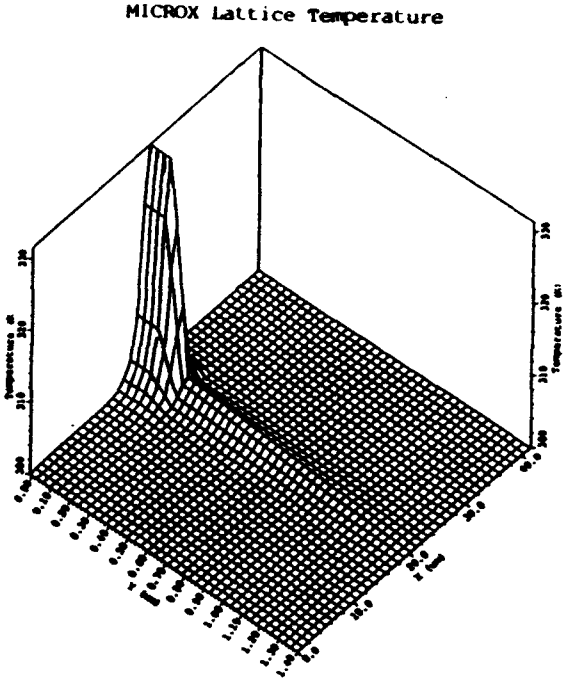


a.

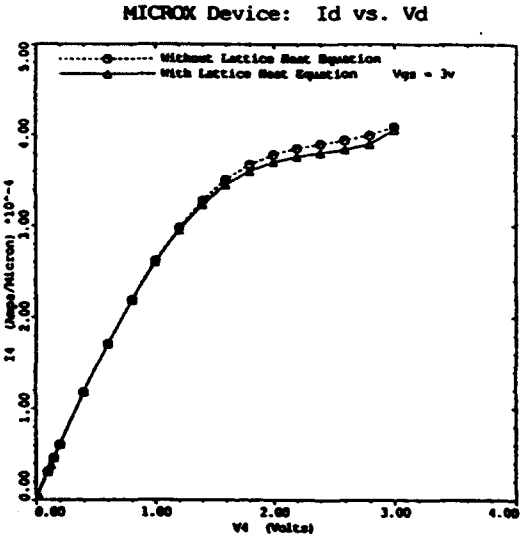


b.

Figure 1. (a.) The maximum rise in channel temperature is 80K for a 10W/cm dissipation level using geometries associated with digital circuits. (b.) A 10% reduction in drain current occurs when lattice heating is included. For this simulation, V_G=3V, the active silicon layer thickness is 1000Å, and the buried oxide thickness is 1000Å.



a.



b.

Figure 2. (a.) The maximum rise in channel temperature is 30K for a 10W/cm dissipation level using geometries associated with microwave monolithic circuits. (b.) A 4% reduction in drain current occurs when lattice heating is included. For this simulation, V_G=3V, active silicon layer thickness is 1000Å, and buried oxide thickness is 1000Å.

APPENDIX D
MICROX PRESENTATION, PUBLICATION

MICROX™ - AN ALL SILICON MICROWAVE TECHNOLOGY

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Published in the 1992 IEEE International SOI Conference
Technical Digest

MICROX™ - An All-Silicon Technology for Monolithic Microwave Integrated Circuits

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Paul G. McMullin, H. C. Nathanson, Michael C. Driver, and
R. Noel Thomas

Published in IEEE Electron Device Letters, Vol. 14, No.5, May 1993

MICROX^{TM} - AN ALL SILICON MICROWAVE TECHNOLOGY

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The MICROX^{TM} concept (MICROWAVE SIMOX$^{®}$), based on the use of very high resistivity (>10^4 ohm-cm) silicon substrates, provides key silicon microwave capabilities in the 1-10 GHz frequency range, namely, low loss microstrip lines, low junction-to-substrate capacitances in FETs, and good isolation between devices [1]. **We have demonstrated this concept with submicron gate complementary FETs (nmos @ 0.25 μm & pmos @ 0.39 μm) having f_{max} values of 32 & 20 GHz in n- and p-channel devices, respectively, with no correction for the parasitic effects of the pads.** These results exceed our previously reported values of 21 and 10 GHz for n and p channel devices, respectively, having similar gate lengths [1]. Thus, the MICROX technology offers all the essential elements for low cost, highly integrable MMICs on silicon substrates and is ready for insertion in L & C band systems. The current research is focused on the integration of CMOS digital control functions with RF circuits (digital attenuator, phase shifter etc.) and the device improvements (e.g. metal T-gate) required for X-band applications.

A critical ingredient of the MICROX technology is the high resistivity silicon substrates (3 and 4 inch diameter) grown in-house by the multiple zone-refining float-zone (FZ) process. Figure 1 shows 4-point probe resistivity data for a typical, as-grown <100> FZ Si crystal along the length. Resistivity values over 40,000 ohm-cm, p-type, indicate extremely low acceptor and donor impurities (~ 10^{12} cm^{-3}). During the high temperature SIMOX anneal, there is some loss of resistivity in about 10 μm thick regions measured from the front and back of the wafer, however the bulk of the wafer remains above 10^4 ohm-cm making it quite suitable for microwave applications up to X-band. In addition, the presence of the 400 nm thick buried oxide helps retain the high resistivity during the subsequent device fabrication.

Our transistor geometry incorporates pads for on-wafer RF probing (Fig. 2). Source pads are interconnected by electroplated gold air-bridges to reduce parasitic capacitance. The final active silicon layer thickness is 120 nm with channel doping of about $2x10^{17}$ cm^{-3}, p- & n-type for n- & p- channel enhancement mode devices, respectively. The electron-beam drawn gate lengths are 0.25 μm (nmos) & 0.39 μm (pmos) ; total width, 4x50 μm; and gate oxide thickness, 12 nm. A self-aligned titanium silicide process with 150 nm nitride side-walls is used on the gate and source/drain regions. To further reduce the gate resistance, the polysilcon gates are re-inforced with 150 nm of gold using a lift-off process. A schematic cross-section of the device is shown in Fig. 3.

Maximum dc g_m values of about 125 & 49 mS/mm are obtained for nmos and pmos FETs, respectively, having low doped drain (LDD) regions (Fig. 4). On-wafer s-parameter data (45 MHz to 26 GHz) were taken using an HP8510B vector network analyzer and RF probes to calculate the maximum stable gain and the maximum available gain (MSG/MAG) (Fig. 5). A typical small-signal equivalent circuit for an n-channel enhancement mode FET is shown in Fig. 6. The small value of the gate resistance reflects the metal reinforcement of the polysilicon gates. Based on this equivalent circuit, our modeling shows that the f_{max} values illustrated in Fig. 5 can be improved up to above 50 & 35 GHz for n- and p-channel devices, respectively, by employing a metal T-gate structure. Finally, with the incorporation of a lateral DMOS structure (to increase the breakdown voltage), and on-chip integration of high speed CMOS digital control functions, the MICROX technology will provide high performance, low cost MMICs from L to X band.

ACKNOWLEDGMENT: The authors would like to acknowledge the support, in part, of this work (contract N00014-91-C-2313) by the Office of Naval Technology *via* the Naval Research Laboratory, Washington, DC.

[1] A. K. Agarwal et al., "MICROX - An Advanced Silicon Technology for Microwave Circuits up to X-Band," in IEDM Tech. Dig., Dec. 1991, p. 687.

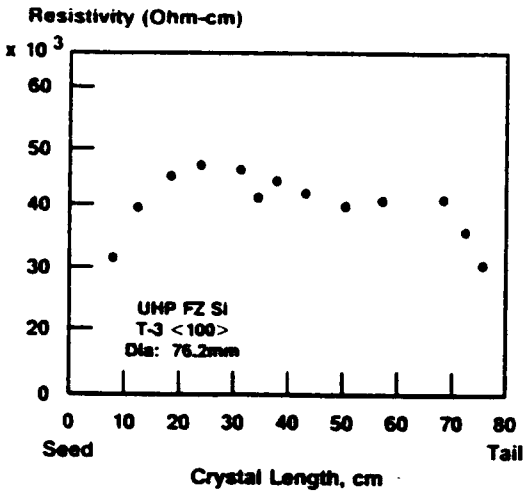

Fig.1 Plot of resistivity vs crystal length for a 3 inch FZ silicon crystal grown in-house.

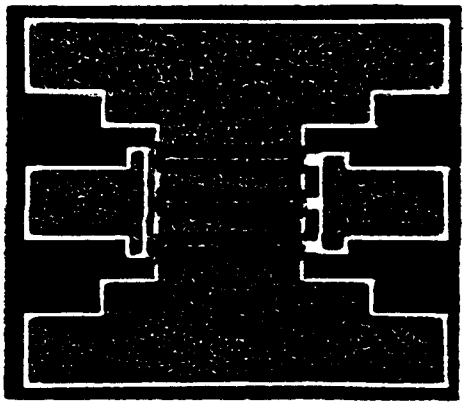

Fig.2 Photomicrograph of a MICROX transistor configured for Cascade probing in common source mode.

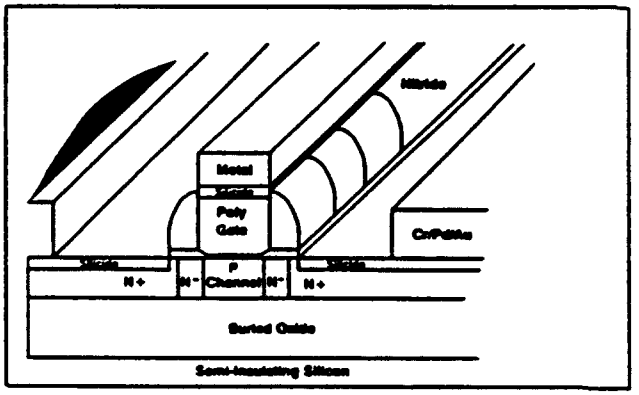

Fig.3 Schematic cross-section of a MICROX nmos FET.

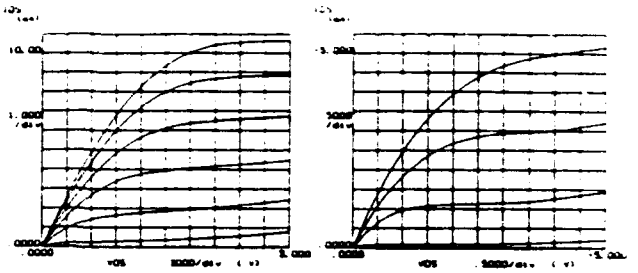

Fig.4 DC characteristics of 2x18 μm wide, nmos (V_g = 0 to 3 V in 0.5 V steps) & pmos (V_g = -2 to -5 V in -1 V steps), enhancement mode MICROX FETs.

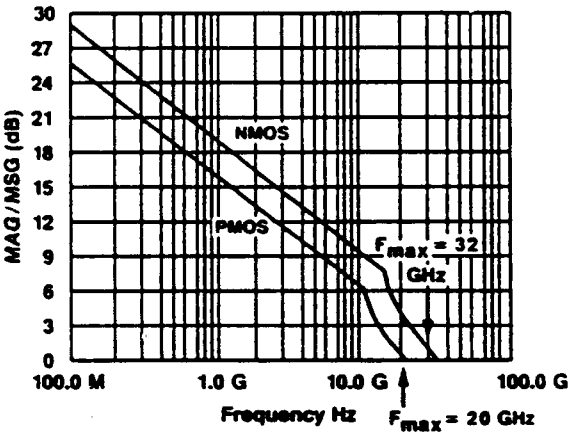

Fig.5 Maximum Available/Stable Gain (MAG/MSG) vs frequency plots obtained from measured s-parameters for the n- & p- channel MICROX FETs with total width of 4x50 μm. The n-channel FET is biased at V_d=3 V, V_g=2 V & I_d=41 mA. and the p-channel FET is biased at V_d=-4 V, V_g=-4 V & I_d=19 mA. The F_{max} values of 32 GHz (nmos) and 20 GHz (pmos) are obtained.

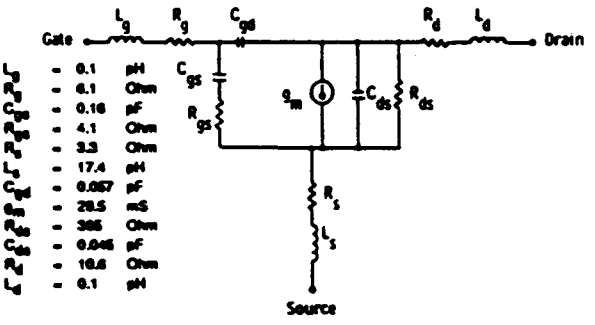

Fig.6 Equivalent circuit obtained for the n-channel MICROX FET of Fig.5. The circuit was extracted by fitting the measured s-parameters up to 26 GHz.

MICROX™—An All-Silicon Technology for Monolithic Microwave Integrated Circuits

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***Abstract*—An improved silicon-on-insulator (SOI) approach offers devices and circuits operating to 10 GHz by providing formerly unattainable capabilities in bulk silicon: reduced junction-to-substrate capacitances in FET's and bipolar transistors, inherent electrical isolation between devices, and low-loss microstrip lines. The concept, called MICROX™ (patent pending), is based on the SIMOX process, but uses very high-resistivity (typically > 10 000 Ω · cm) silicon substrates. MICROX NMOS transistors of effective gate length (0.25 μm) give a maximum frequency of operation, f_{max}, of 32 GHz and f_T of 23.6 GHz in large-periphery (4 × 50 μm) devices with no correction for the parasitic effects of the pads. The measured minimum noise figure is 1.5 dB at 2 GHz with associated gain of 17.5 dB, an improvement over previously reported values for silicon FET's.**

I. Introduction

HISTORICALLY, silicon and GaAs devices have served separate circuit and systems needs. Silicon devices have not been available for monolithic integration in microwave applications above 1 GHz due to low carrier mobility in surface channel FET's, parasitic capacitances in conventional bulk transistors, and the lack of a high-resistivity substrate to support low-loss microstrip lines. Without these technical limits, GaAs has provided a means to realize monolithic microwave integrated circuits (MMIC's). For GaAs, however, circuit costs are high due to limited wafer sizes. Furthermore, prospects for extensively integrating digital and RF functions in GaAs are remote, given the unavailability of CMOS GaAs circuitry. Strong needs exist for affordable high-speed/frequency circuits combining digital and RF capabilities in such areas as phased array radars and in supercomputers.

The MICROX (*micro*wave SIM*OX*) concept presented in this paper is an advance over conventional SIMOX (*si*licon isolated by *im*planted *ox*ygen). It removes the conventional constraints of bulk silicon technology, allowing improved microwave FET performance. Similar improvements are expected for bipolar and CMOS digital devices using MICROX.

Recent RF results for silicon-on-insulator (SOI) and bulk silicon FET's are encouraging [1]–[3], but the modest FET widths used (25–60 μm) significantly limit power compared to typical GaAs microwave FET's (200–600 μm). Silicon-on-sapphire (SOS) FET's (0.3-μm-thick Si, effective gate length = 0.35 μm and no LDD region, width = 2 × 25 μm, Al T-gates reinforcing polysilicon gates) have given unilateral gain cutoff frequency (f_{max}) values of 53 and 37 GHz for n- and p-channel devices, respectively [1]. The values of f_T for n- and p-channel devices were 23 and 20 GHz, respectively. No minimum noise figure was reported. Drawbacks to this approach are the lack of high-quality, large-diameter SOS substrates and the difficulty of SOS wafer processing. With 50-Ω · cm resistivity silicon substrates, f_{max} values of 14 GHz have been reported on bonded and etched back silicon-on-insulator (BESOI) wafers for small NMOS transistors (gate length = 1 μm, width = 2 × 60 μm, no metal gate) [2]. Minimum noise figure for these BESOI devices was 5.0 dB at 2 GHz; associated gain was 6.4 dB. The reported f_{max} values required correction for contact pad parasitics, due to effects of the 50-Ω · cm substrate resistivity. Recently, bulk NMOS devices (50-Ω · cm substrate, gate length = 0.5 μm, width = 2 × 25 μm, no metal gate) were reported with f_{max} = 21 GHz, but only after correction for the pad capacitances [3], again because of the substrate resistivity. Minimum noise figure was 5.3 dB at 8 GHz; associated gain was 4.6 dB.

In this paper, we report high-frequency results for large-periphery CMOS MICROX devices fabricated on substrates having initial resistivity values of about 10 000 Ω · cm. Values of f_{max} were 32 GHz for large NMOS transistors (effective gate length = 0.25 μm, width = 4 × 50 μm, metal reinforced polysilicon gates). There was no need to separately extract the parasitic effects of the microwave probe contact pads, due to the high substrate resistivity. The minimum noise figure was 1.5 dB at 2 GHz and 3.25 dB at 8 GHz; associated gain was 17.5 dB at 2 GHz and 8.5 dB at 8 GHz.

Manuscript received June 24, 1992; revised February 11, 1993. This work was supported in part by the Office of Naval Technology via the Naval Research Laboratory, Washington, DC.

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IEEE Log Number 9208393.

0741-3106/93$03.00

II. The MICROX Concept

For MICROX, the SIMOX process is used on a very high-resistivity (typically > 10 000 Ω · cm) float-zone silicon substrate (Fig. 1), to combine the advantages of the SIMOX structure (reduced source and drain capacitances, higher transconductance, and dielectric isolation) with the benefits of a high-resistivity substrate (decoupling of interelectrode capacitances within active devices, low-loss microstrip lines, and high-Q passive components). With the MICROX approach, all the essential elements for low-cost, highly integrable MMIC's can be obtained using silicon substrates and processing methods. Also, cointegration of high-speed CMOS digital circuitry is possible.

The high-resistivity silicon crystals (3 and 4 in diameter) used for this work are grown in-house by the multiple zone-refining float-zone (FZ) process using ultrahigh-purity polysilicon rods. Fig. 2 shows the radial plot of four-point probe resistivity typical of ⟨100⟩ FZ Si substrates [4], [5]. Extremely low acceptor and donor impurities ($\sim 10^{12}$ cm^{-3}) are indicated by resistivity values exceeding 40 000 Ω · cm, p-type. Measured photoconductive decay lifetime values of 6 to 10 ms for these crystals indicate very low concentrations ($\leq 10^{10}$ cm^{-3}) of deep levels, confirming the high purity of these starting crystals.

III. Special Device Features

The MICROX transistors used an adapted microwave GaAs MESFET design with pads for on-wafer coplanar microwave probing. Source regions were interconnected by electroplated gold air-bridges to reduce parasitic resistance, inductance, and capacitance [6]. The active silicon layer thickness was 120 nm with channel doping $\sim 2 \times 10^{17}$ cm^{-3}, p-type, for n-channel enhancement-mode FET's. Electron-beam exposure defined a 0.35-μm-long gate, with a total width of 4 × 50 μm. The gate oxide was 12 nm thick. A self-aligned titanium silicide process with 150-nm nitride gate sidewalls (formed after the LDD implant) was used to lower the resistance of the gate and source/drain regions. A 150-nm-thick chrome/palladium/gold layer reinforced the wide, submicrometer-long polysilicon gates to further reduce the gate resistance.

IV. DC and Microwave Measurements

N-channel FET's (0.25-μm effective gate length) with low doped drain (LDD) regions had a maximum dc transconductance of 125 mS/mm. On-wafer s-parameter measurements (0.045 to 26 GHz), made with an HP 8510B vector network analyzer and Cascade microwave probes, were used to calculate the maximum stable gain (MSG) and the maximum available gain (MAG) [6]. Results for both n- and p-channel FET's are shown in Fig. 3. The frequency at which MAG = 0 dB (f_{max}) was 32 GHz for the n-channel FET and 20 GHz for the p-channel one. The values of f_T for n- and p-channel devices were 23.6 and 9.2 GHz, respectively. The s-parameter data were also used to extract small-signal equivalent circuits, employing the microwave analysis program Touchstone©. A typical equivalent n-channel circuit result is shown in Fig. 4. The low equivalent gate resistance confirms the value of reinforcing the wide polysilicon gates with metal. Measurements on n-channel FET's made with an HP 8970B noise figure meter gave a minimum noise figure of 1.5 dB at 2 GHz and 3.25 dB at 8 GHz with associated gain of 17.5 dB at 2 GHz and 8.5 dB at 8 GHz, an improvement over the results for BESOI and SIMOX devices discussed

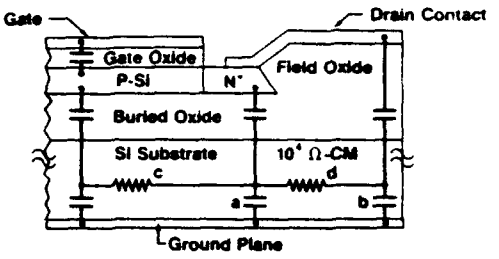

Fig. 1. A schematic of the device cross section showing buried oxide and substrate parasitic capacitances in an n-channel MICROX FET. The high resistivity of the substrate not only reduces junction and pad capacitances (indicated at a and b) but also decouples (as indicated at c and d) key substrate parasitic capacitances that limit the frequency of operation.

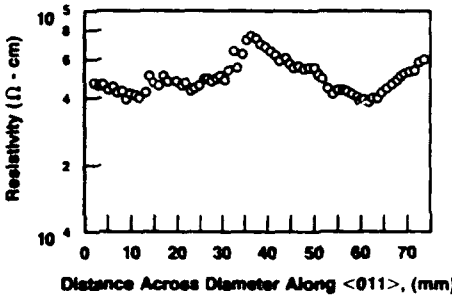

Fig. 2. A plot of the resistivity along the ⟨011⟩ direction of an ultrahigh-purity float-zone silicon wafer.

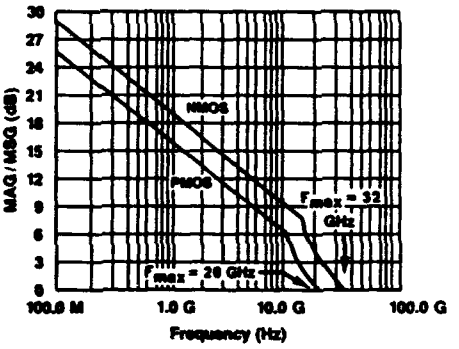

Fig. 3. Plots of MAG/MSG versus frequency obtained from measured s-parameters for n-channel and p-channel MICROX FET's. Pertinent values: n-channel (p-channel) effective gate length of 0.25 μm (0.40 μm) and width of 4 × 50 μm (4 × 50 μm). For bias at V_d = 3 V (−4 V), V_g = 2 V (−4.0 V), and I_{ds} = 41 mA (−19 mA), the values of f_{max} and f_T were 32 GHz (20 GHz) and 23.6 GHz (9.2 GHz), respectively.

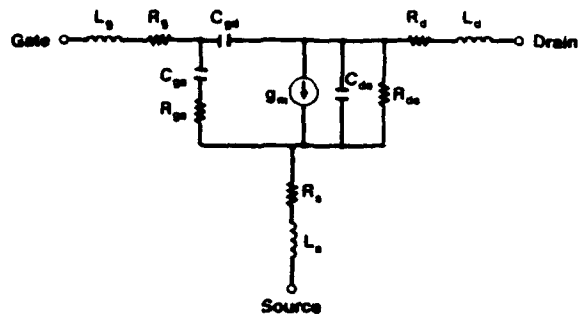

Fig. 4. Equivalent circuit for an n-channel MICROX FET with L_{eff} = 0.25 μm, W = 4 × 50 μm, V_d = 3 V, V_g = 2 V, and I_{ds} = 41 mA. The following parameter values were extracted by fitting the measured s parameters up to 26 GHz: L_g = 0.1 pH, R_g = 4.1 Ω, C_{gs} = 0.16 pF, R_{gs} = 1.0 Ω, R_s = 1.1 Ω, L_s = 17.4 pH, C_{gd} = 0.057 pF, g_m = 29.5 mS, C_{ds} = 0.045 pF, R_{ds} = 305 Ω, R_d = 10.6 Ω, and L_d = 0.1 pH.

in Section I. The minimum noise figure for p-channel devices was 2.7 dB at 2 GHz with associated gain of 14.7 dB.

V. Conclusion

With an f_{max} value of 32 GHz, wide-periphery NMOS transistors of submicrometer gate length demonstrate the viability of the MICROX concept for silicon microwave use. Retention of substrate resistivity adequate for microwave performance after complete device processing is confirmed; no separate decoupling of contact pad capacitance from the active device is required. Further improvements in the f_{max} value and the minimum noise figure will result from a) reinforcing a submicrometer polysilicon gate with a superimposed metal T-gate as was done in [1], and b) using a thinner silicon channel layer for fully depleted operation to increase g_m by at least 20%. A lateral DMOS structure as described in [7] will provide higher breakdown voltage without sacrificing f_{max}.

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